[UNIT - 1]

Understand the Construction & Working of Power Electronic Devices

1. Understand the Construction and Working of Power Electronic Devices

- 1.1 Construction, Operation, V-I Characteristics & Application of Power Diode, SCR, DIAC, TRIAC, Power MOSFET, GTO & IGBT
- 1.2 Two Transistor Analogy of SCR.
- 1.3 Gate Characteristics of SCR.
- 1.4 Switching Characteristic of SCR during Turn ON and Turn OFF.
- 1.5 Turn ON Methods of SCR.
- 1.6 Turn OFF Methods of SCR (Line Commutation and Forced Commutation)
  - 1.6.1 Load Commutation
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  - 1.9.5 Synchronous triggering (Ramp Triggering)
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❖ INTRODUCTION : -

- Power Electronics belongs to partly to Power Engineering & partly to Electronics Engineering.
- **Power Engineering** is mainly concerned with Generation, Transmission, Distribution and Utilization of Electric Energy at High efficiency.
- **Electronics Engineering** is guided by distortion less production, transmission and reception of data and signals of very low power level, of the order of a few watts, or milliwatts, without much consideration to the efficiency.
- **Power Engineering** is based on electromagnetic principle where as **Electronics Engineering** is based upon Physical phenomena in Vacuum, gases or semiconductors.
- **Power Electronics** is a subject that deals with the apparatus and equipment working on the principle of electronics but rated at power level rather than signal level.
- For example, semiconductor power switches such as Thyristors, GTOs etc work on the principle of electronics (movement of holes & electrons) but have the name attached to them only as a description of their power ratings.

❖ APPLICATION OF POWER ELECTRONICS: -

- ♣ Aerospace (Space shuttle power supply, satellite power supply, aircraft power supply etc.)
- ♣ Commercial (Heating, Air-conditioning, Refrigeration, UPS, Elevator, Light Dimmers, Flashers etc.)
- ♣ Industrial (Arc Furnaces, Blowers, Pumps, Compressors, Rolling mills, welding, textile mills, cement mills etc.)
- ♣ Residential (Air-conditioning, Lighting, refrigerator, vacuum cleaner, washing machines, food mixers etc.)
- ♣ Telecommunication (Battery Chargers, Power Supplies, UPS etc)
- ♣ Transportation (Traction control of electric vehicles, electric locomotives, street cars, trolley buses etc)
- ♣ Utility Systems (High Voltage DC Transmission<HVDC>, excitation systems, static circuit breakers etc)

❖ ADVANTAGES POWER ELECTRONICS: -

- ♣ High efficiency due to low loss in power semiconductor devices.
- ♣ High reliability of power electronic converter systems.
- ♣ Long life and less maintenance due to absence of any moving parts.
- ♣ Fast dynamic response of the system as compared to electromechanical systems.
- ♣ Small size and less weight results in less floor space and less installation charge.
- ♣ Mass production of power semiconductor devices has resulted in lower cost of equipments.

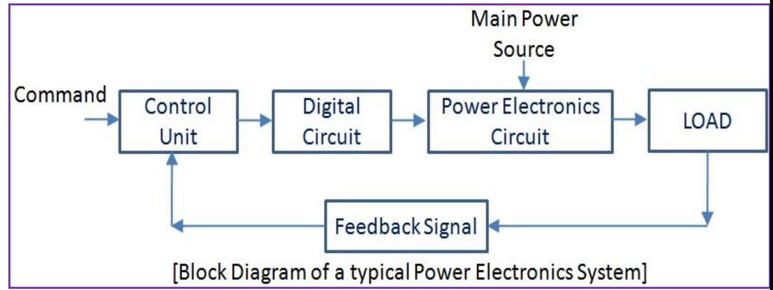
❖ DISADVANTAGES POWER ELECTRONICS: -

- ♣ Regeneration of power is difficult in power electronics converter systems.
- ♣ Power electronics controllers have low overload capacity. So cost of controller may increases.

✓ *But the advantages possed by powe electronics faor weight then disadvantages mentioned above.*

❖ POWER ELECTRONICS SYSTEMS: -

- The major components of a power electronics system are shown in the form of a block diagram below.
- Main power sources may be an ac supply or dc supply system.
- The output from the power electronics circuit may be variable dc, or ac voltage, or it may be a variable voltage and frequency.
- In general, the output of a power electronics converter circuit depends upon the requirements of the load.
- The feedback components measures a parameter of the load, say speed in case of a rotating machines and compares it with the command.



[Block Diagram of a typical Power Electronics System]

- The difference of the two through the digital circuit components, controls the instant of turn-on of semiconductor devices forming the solid state power converter systems.
- In this manner, behavior of the load circuit can be controlled, as desired, over a wide range with the adjustment of the command.

❖ SOME SYMBOLS OF POWER SEMICONDUCTOR DEVICES: -

DEVICE	CIRCUIT SYMBOL	DEVICE	CIRCUIT SYMBOL
Power Diode	Anode (+), Cathode (-)	TRIAC (Triode for Alternating Current)	MT 1, GATE, MT 2
SCR (Silicon Controlled Rectifier)	Anode, Gate, Cathode		
DIAC (Diode for Alternating Current)	T1, T2	BJT (Bipolar Junction Transistor)	NPN: B, C, E; PNP: B, E, C
GTO (Gate-Turn Off Thyristor)	A, K, G; A, K, G		
IGBT (Insulated Gate Bipolar Transistor)	C, G, E	MOSFET (Metal Oxide Semiconductor Field Effect Transistor)	G, D, S; G, S, D
LASCR (Light Activated SCR)	A, K, G	MCT (MOS Controlled Thyristor)	A, G, K
ASCR/RCT (Asymmetric SCR/ Reverse Conducting Thyristor)	A, K, G	SIT (Static Induction Transistor)	D, G, S

❖ TYPES OF POWER ELECTRONICS CONVERTERS: -

- **Diode Rectifiers** (Converts Input AC Voltage into Fixed DC Voltage)
- **Phase Controlled Rectifiers** (Convert Constant AC Voltage into Variable DC output Voltages)
- **DC Choppers** (Converts Fixed DC input Voltage into a Controllable DC output Voltages)
- **Inverters** (Converts Fixed DC Voltages into Variable AC Voltages)
- **Cycloconverter** (Converts input power at one frequency to output power at different frequency;ac→ac)
- **Static Switches** (AC Static Switch or DC Static Switch)

Ψ Power Semiconductor devices are classified into **3** categories according to degree of controllability

- Un Controlled Turn ON and Un Controlled Turn OFF Devices. < Ex – Diode >
- Controlled Turn ON and Un Controlled Turn OFF Devices. < Ex – SCR >
- Controlled Turn ON and Controlled Turn OFF Devices. < Ex – BJT, MOSFET, GTO etc >

POWER DIODE: -

- A low-power Diode, called Signal Diode, is a p-n junction device.
- A high-power diode, called Power Diode, is also a p-n junction device but with constructional feature is different from a signal diode.
- Voltage, current & power rating of Power Diodes are much higher than the rating of Signal Diodes.

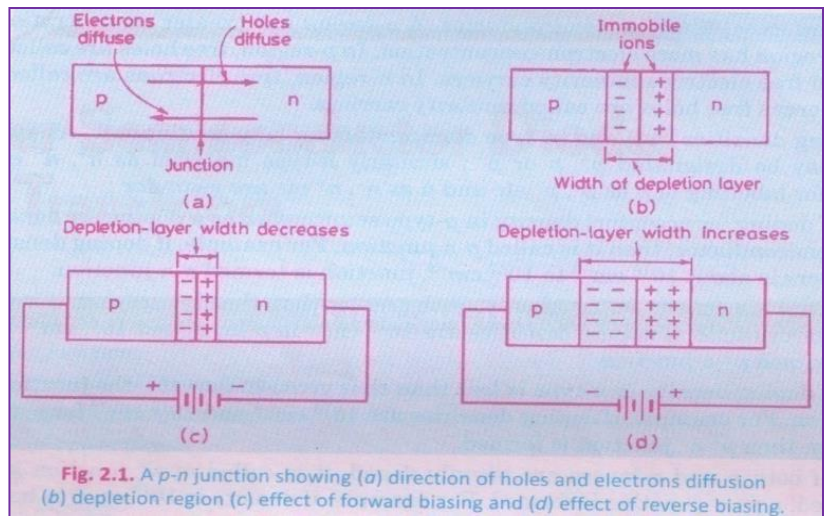


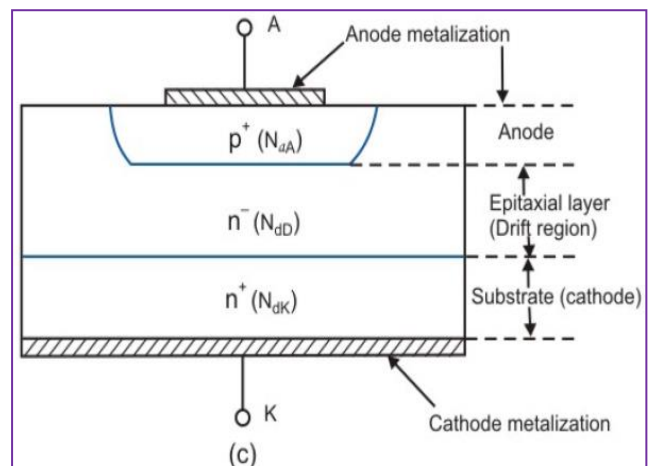
Fig. 2.1. A *p-n* junction showing (*a*) direction of holes and electrons diffusion (*b*) depletion region (*c*) effect of forward biasing and (*d*) effect of reverse biasing.

Ψ P-N Junction

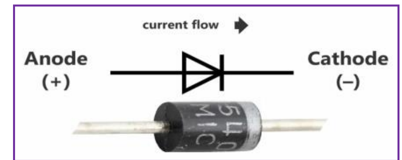
- A p-n junction forms the basic building block of all power semiconductor devices. A p-n junction is formed when a p-type semiconductor is bought in physical contact with n-type semiconductor.
- Doping densities in p and n type semiconductors may be different. As such, p-type material may be designated as **p^+, p or p-** ; similarly n-type material may be designated as **n^+, n or n-** etc.
- If doping (acceptor) density in p-type semiconductor = doping (donor) density in n-type semiconductor, then it is called **p-n** junction.
- If doping density in p-type region is much greater than that in n-region, then it is called **p^+ n** junction.
- If doping density in n-type region is less than that in p-region, then it is called **p n^-** junction.
- If both p and n layers are heavily doped, it is called **p^+ n^+** junction and if both p and n layers are lightly doped, it is called **p^- n^-** junction is formed.
- In general, **p^+** indicated highly doped p region, **n^-** indicated lightly doped n region and so on.

Ψ Construction Structure Of Power Diode: -

- Power Diodes differ in structure from signal diodes.
- A signal diode simple constitutes a simple p-n junction as shown in figure above.
- The detail in constructing power diode arises from the need to make them suitable for high-voltage and high current applications.
- Thus a power diode should be so designed as to handle high forward current and large reverse breakdown voltages. The practical realization and the resulting structure of a power diode is in figure.



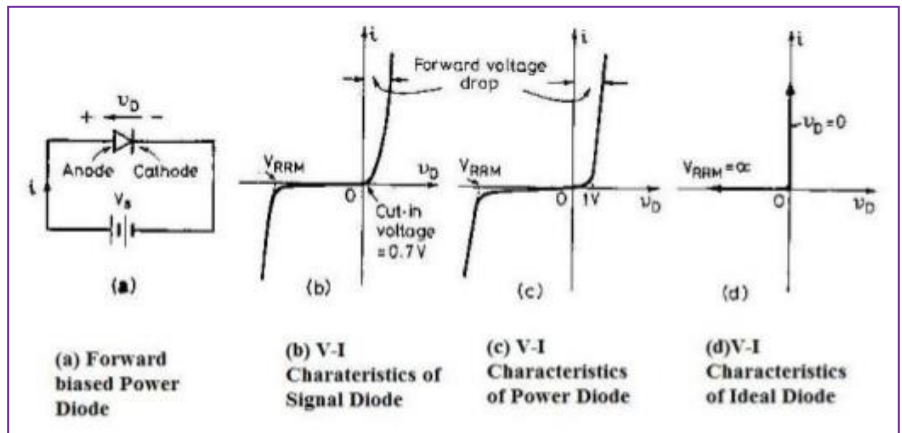
- It consists of heavily doped n^+ substrate. On this structure, a lightly doped n^- layer is epitaxial grown.
- Now a heavily doped p^+ layer is diffused into n^- layer to form the anode of power diode. Figure shows that n^- layer is the basic structural feature not found in signal diodes. The structure of n^- layer is to absorb the depletion layer of the reverse biased $p^+ n^-$ junction J_1.



- The breakdown voltage needed in a power diode governs the thickness of n^- layer; greater the breakdown voltage, more the n^- layer thickness. This n^- layer is lightly doped, nearly intrinsic.
- Because of this reason, n^- layer is sometimes called i-layer & the device as p-i-n or PiN diode.
- The drawback of n^- layer is to add significant ohmic resistance to the diode when it is conducting a forward current. This leads to large power dissipation in the diode; so proper cooling arrangements in large diode ratings are essential. The circuit symbol of a power diode is same as that for a signal diode.

Ψ V-I Characteristics Curve Of Power Diode: -

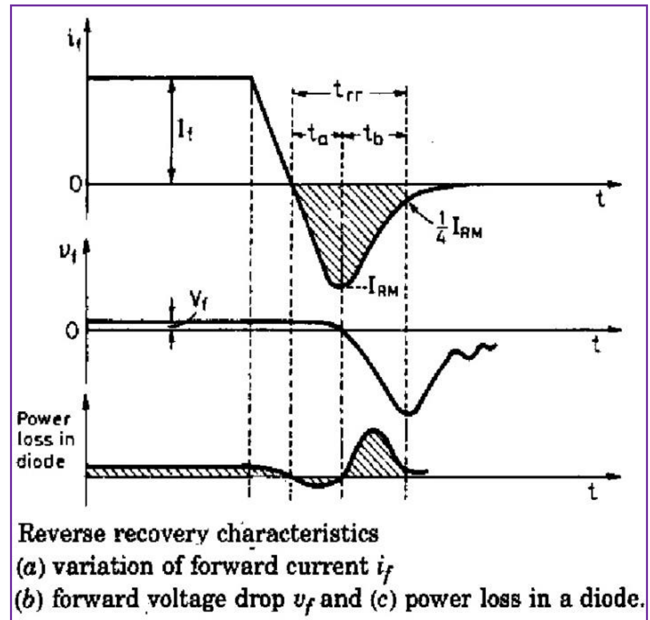
- Power diode is a two terminal p-n semiconductor device.
- The two terminals of diode are called Anode and Cathode.
- The important characteristics of power diodes are described here:
- When anode is positive with respective to cathode, diode is said to be **Forward Biased**.
- With increase of the source voltage V_s from zero value, initially diode current is zero. From $V_s = 0$ to cut-in voltage, the forward-diode current is very small.



(a) Forward biased Power Diode (b) V-I Charateristics of Signal Diode (c) V-I Characteristics of Power Diode (d)V-I Characteristics of Ideal Diode

- Cut-in voltage is also known as threshold voltage or turn-on voltage. Beyond cut-in voltage, the diode current rises rapidly and the diode is said to conduct. For silicon diode, the cut-in voltage is around 0.7V. When diode conducts, there is a forward voltage drop of the order of 0.8 to 1V.
- For low-power diodes, current in the forward direction increases first exponentially with voltage and then becomes almost linear as shown in fig (b).
- For power diode, the forward current grows almost linearly with voltage as shown I fig (c).
- The high magnitude of the current in a power diode leads to ohmic drops that hide the exponential part of V-I curve. The n^- or drift region forms a considerable drop in the ohmic resistance of power diodes.
- When cathode is positive with respective to anode, the diode is said to be **Reverse Biased.**
- In this condition, a small reverse current called leakage current, of the order of μA flows.
- The leakage current is almost independent of the magnitude of reverse voltage until this voltage reaches breakdown voltage. At this reverse breakdown, voltage remains almost constant but reverse current becomes quite high - limited only by the external circuit resistance.
- A large reverse breakdown voltage associated with high reverse current, leads to excessive power loss that may destroy the diode. This shows that reverse breakdown of a power diode must avoided by operating it below the specific peak reverse repetitive voltage $\mathbf{V_{RRM}}$.
- Fig. (c) Shows that the V-I characteristics and V_{RRM} of a power diode.
- For an Ideal Diode the V-I characteristic is shown in Fig. (d). Here voltage drop across conducting diode, $v_D = 0$, reverse leakage current = 0, cut-in voltage = 0 and reverse breakdown voltage $V_{RRM} = \infty$.
- Diode manufactures also indicate the value of Peak Inverse Voltage (PIV) of a diode.
- This is the largest reverse voltage to which a diode may be subjected during its working.
- PIV is same as V_{RRM}.

Ψ Diode Reverse Recovery Characteristics: -



Reverse recovery characteristics
(*a*) variation of forward current i_f
(*b*) forward voltage drop v_f and (*c*) power loss in a diode.

- After the forward diode current decays to zero, the diode continues to conduct in the reverse direction because of the pressure of stored charges in the depletion region and the semiconductor layers.
- The reverse current flows for a time called *reverse recovery time* (**t_{rr}**).
- The diode regains its blocking capability until reverse recovery current decays to zero.
- The *reverse recovery time* (t_{rr}) is defined as the time between the instant forward diode current becomes zero & instant recovery current decays to 25% of its reverse peak value I_{RM} as shown in fig(a).
- The reverse recovery time is composed of two segments of time t_a and t_b i.e $\mathbf{t_{rr} = t_a + t_b}$.
- Time **t_a** is the time between zero crossing of forward current and peak reverse current I_{RM}.
- During the time t_a, charge stored in depletion layer is removed.
- Time **t_b** is measured from the instant of reverse peak value I_{RM} to the instant when 0.25 I_{RM} is reached.
- The ration of **t_b/t_a** is called **softness factor** or S-factor.
- This factor is a measure of the voltage transistors that occur during the time diode recovers.
- Its usual value is unity and indicates low oscillatory reverse recovery process.
- In case S-factor is small, diode has large oscillatory over voltage.
- A diode with S-factor = **1** is called *soft-recovery diode* & a diode with S-factor < **1** is called *snappy-recovery diode* or *fast-recovery diode*.
- Fig. (b) shown the waveform of forward-voltage drop v_f across the diode.
- The product of v_f and i_f gives the power loss in a diode. Its variation is shown in fig.(c).
- Fig (c) shows that the major power loss in a diode occurs during the period of t_b. $I_{RM} = t_a$ x (di/dt).

Ψ APPLICATIONS: -

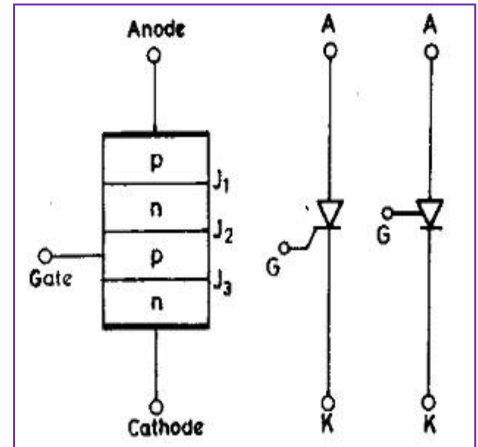
- ♣ Battery Charging
- ♣ UPS
- ♣ Switching Power Supply
- ♣ Electroplating
- ♣ Welding

THYRISTOR : -

- The term Thyristor is derived from the word of **Thyr**atron (a gas fluid tube work as SCR) & Trans**istor**
- This means that Thyristor is a solid state device like a transistor and has characteristics similar to that of a thyratron tube.
- It is a two to four lead solid state semiconductor device with four layers of alternating n and p type material. Thyristors are controlled devices. It is also known as **PNPN** device.
- They are operated as bistable switches i.e. operating from non conducting state to conducting state.
- It has two stable states i.e. ON and OFF state and it can change from one state to another.
- Some of the **Thyristor Families** are : -
  - ♣ **SCR** (Silicon Controlled Rectifier)
  - ♣ **DIAC** (Diode for Alternating Current)
  - ♣ **TRIAC** (Triode for Alternating Current)
  - ♣ **GTO** (Gate-Turn Off Thyristor)
  - ♣ **IGBT** (Integrated Gate Bipolar Transistor)
  - ♣ **UJT** (Uni-Junction Transistor)
  - ♣ **LASCR** (Light Activated SCR)
  - ♣ **ASCR** (Asymmetric SCR)
  - ♣ **RCT** (Reverse Conducting Thyristor)
  - ♣ **SIT** (Static Induction Transistor)
  - ♣ **SITH** (Static Induction Thyristor)
  - ♣ **MCT** (MOS Controlled Thyristor)
  - ♣ **PUT** (Programmable Unijunction Transistor)
  - ♣ **SUS** (Silicon Unilateral Switch)

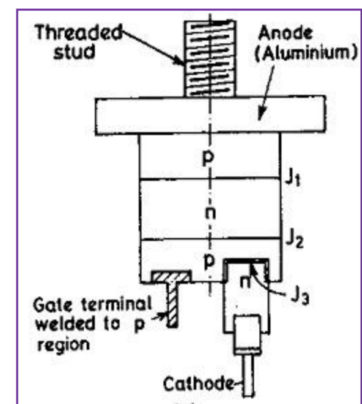
- **SBS** (Silicon Bilateral Switch)
- **SCS** (Silicon Controlled Switch)
- **LASCS** (Light Activated SCS)
- **GATE** (Gate Assisted Turn Off Thyristor)
- **MTO** (MOS Turn-OFF Thyristor)
- **ETO** (Emitter Turn-OFF Thyristor)

SCR <Silicon Controlled Rectifier>: -

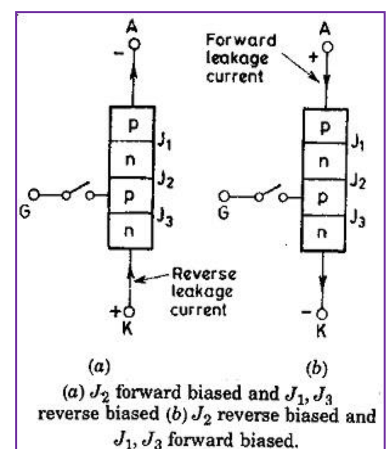


- The structure & symbol of the Thyristor (SCR) are shown in fig.
- It is a **Four Layered** PNPN switching device, having **Three Junctions** J_1, J_2, & J_3. It has **Three Terminals**, namely Anode (A), Cathode (K) and Gate (G).
- The Anode & Cathode are connected to the main power circuit.
- The Gate terminal carries a low level gate current in the direction gate to cathode. Normally, the gate terminal is provided at the P layer near the cathode. This is known as Gate.
- A SCR is so called because Silicon is used for its construction and its operation as a rectifier and it can be controlled.
- Like diode, SCR is a unidirectional device that blocks the current from cathode to anode. Unlike diode is a SCR also blocks the current flow from anode to cathode until it is triggered by proper gate signal.

Ψ Operation of SCR: -

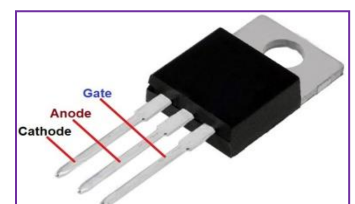


- When the end P Layer is made positive with respect to the end N Layer, the outer junctions, J_1 and J_3 are forward biased but the middle layer J_2 becomes reverse biased.
- Thus the junction J_2 because of the presence of depletion layer, does not allow any current to flow through the device. Only leakage current, negligibly small in magnitude, flows through the device due to drift of the mobile charges. This current is insufficient to make the device conduct.
- The depletion layer, mostly of immobile charges does not constitute any flow of current. In other word, the SCR under the forward biased condition does not conduct. This is called as **Forward Blocking State** or **Off State** of the device.
- When the end n layer is made positive with respect to end p layer, the middle Junction J_2 becomes forward biased whereas the two outer junctions, J_1 and J_3 become reverse biased. The Junctions J_1 and J_3 do not allow any current to flow through the device. Only a very small amount of leakage current may flow because of the drift of the charges.
- The leakage current is again insufficient to make the device conduct.
- This is known as the **Reverse Blocking State** or **Off-State** of the device.



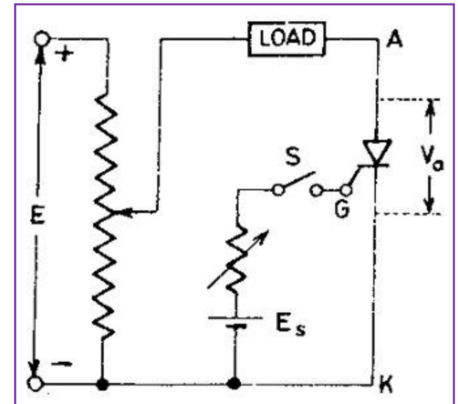
(a) J_2 forward biased and J_1, J_3 reverse biased (b) J_2 reverse biased and J_1, J_3 forward biased.

- The width of the depletion layer at the junction J_2 decreases with the increase in anode to cathode voltage (since the width is inversely proportional to voltage).
- If the voltage between the anode and cathode is kept on increasing, a stage comes (corresponding to forward break over voltage) when the depletion layer at J_2 vanishes.
- The reverse biased junction J_2 will breakdown due to the large voltage gradient across its depletion layer. This phenomenon is known **Avalanche Break Down**.



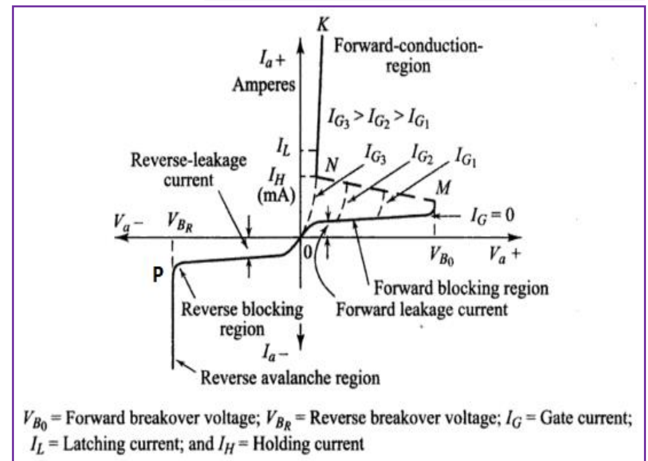
- Since the other junctions, J_1 and J_3 are already forward biased there will be a free carrier movement across all the three junctions resulting in a large amount of current flowing through the device from anode to cathode.
- Due to the flow of this forward current, the device starts conducting and is then said to be in the **Conducting state** or **On State.**

Ψ Static Anode-Cathode <V-I> Characteristics of SCR: -



- An elementary circuit diagram for obtaining static V-I characteristics of the Thyristor (SCR) is in Fig.
- Here, the anode and cathode are connected to the main source through a load. The gate & cathode are fed from another source E_g.
- The static V-I characteristic of an SCR is shown in Fig.
- Here, V_a is the anode-cathode voltage and I_a is the anode current.
- The Thyristor V-I characteristics is divided into three regions of operation. These three regions of operation are described below : -

♣ Reverse Blocking Region: -



V_{B_0} = Forward breakover voltage; V_{B_R} = Reverse breakover voltage; I_G = Gate current; I_L = Latching current; and I_H = Holding current

- When the cathode is made positive with respect to anode with the switch S open (Fig.1), the Thyristor becomes reverse biased.
- In Fig.2 OP is the reverse blocking region.
- In this region, the Thyristor exhibits a blocking characteristic similar to that of a diode.
- In this reverse biased condition, the outer junction J_1, and J_3 are reverse biased and the middle junction J_2 is forward biased.
- Thus, only a small leakage current (in mA) flows.
- If the reverse voltage is increased, then at a critical breakdown level called **reverse breakdown voltage** V_{BR}, an avalanche will occur at J_1 and J_3 increasing the current sharply.
- If the current is not limited to a safe value, power dissipation will increase to a dangerous value that may destroy the device. Region PQ is the reverse avalanche region.
- If the reverse voltage applied across the device is below this critical value, the device will behaves as a high-impedance device (i.e., essentially open) in the reverse direction.
- The inner two regions of the SCR are lightly doped compared to the outer layers.
- Hence, the thickness of the J_2 depletion layer during the forward biased conditions will be greater than the thickness of the depletion layers at J_1 and J_3 when the device is reverse biased.
- **Thus**, forward break-over voltage V_{BO} is generally higher than the reverse break-over voltage V_{BR}.

♣ Forward Blocking Region: -

- In this region, the anode is made positive with respect to the cathode and therefore, junctions J_1 and J_3 are forward biased while the junction J_2 remains reverse biased.
- Hence, the anode current is a small forward leakage current. The region OM of the V-I characteristic is known as the forward blocking region when the device does not conduct.

♣ Forward Conduction Region : -

- When the anode to cathode forward voltage is increased with the gate circuit kept open, avalanche breakdown occurs at the junction J_2 at a critical forward break-over voltage (V_{BO}), and the SCR switches into a low impedance condition (high conduction mode).
- In Fig. the forward breakover voltage is corresponding to the point M, when the device latches on to the conducting state.
- The region MN of the characteristic shows that as soon as device latches on to its ON state, the voltage across the device drops from say, several hundred Volts to 1-2 Volt, depending on rating of the SCR, and suddenly a very large amount of current starts flowing through the device.
- The part NK of the characteristic is called as the forward conduction state.

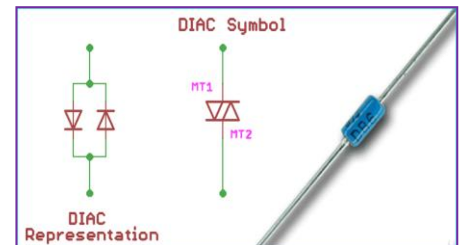
- In this high conduction mode, the anode current is determined essentially by the external load impedance. Thus when the Thyristor conducts forward current, it can be regarded as a closed switch.
- When a gate-signal is applied, the Thyristor turns-on before V_{BO} is reached.
- The forward voltage at which the device switches to ON state depends upon the magnitude of gate current; higher the gate current, lower is the forward breakover voltage.
- Figure shows that for gate current $I_G = 0$, the forward breakover is V_{BO}.
- For I_{G1}, the forward breakover voltage is less than V_{BO} and for $I_{G2} > I_{G1}$, it is still further reduced.
- In practice, the magnitude of gate-current more than the minimum gate current required to turn-on the SCR. The typical gate current magnitudes are of the order of 20 to 200 mA.
- Once the SCR is conducting a forward current that is greater than the minimum value, called the **Latching Current**, the gate signal is no longer required to maintain the device in its ON state.
- Removal of the gate current does not affect the conduction of the anode current.
- The SCR will return to its original forward blocking state if the anode current falls below a low level, called the **Holding Current** (I_H). For most industrial applications, this holding current (typically 10 mA) can be regarded as being essentially zero.
- Note that latching current is associated with turn-on process and holding current with turn-off process.
- The holding current is usually lower than, but very close the latching current.
- Hence, from the above discussion it becomes clear that the more convenient, reliable and efficient method of turning on the device employs the gate drive.

Ψ Applications of SCR

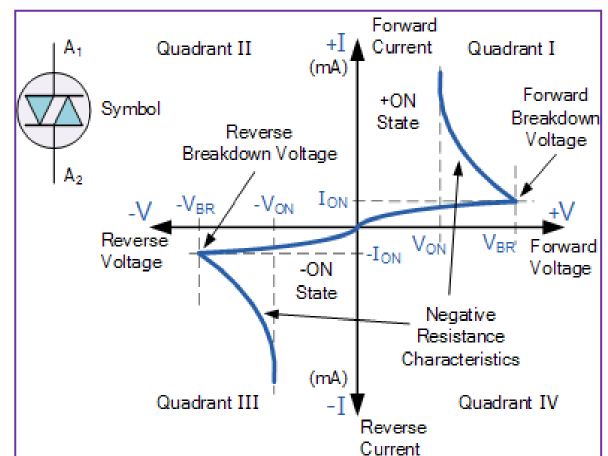
- Power Control
- Switching
- Zero Voltage Switching
- Over-Voltage Protection
- Pulse Circuits
- **Battery Charging Regulator**

DIAC < Diode for Alternating Current **or** Bidirectional Diode Thyristor >

- It DIAC is a two electrode, bidirectional avalanche diode which can be switched from the off-state to the on-state for either polarity of applied voltage.
- The schematic construction, V-I characteristics and circuit symbol of DIAC is shown in figure.

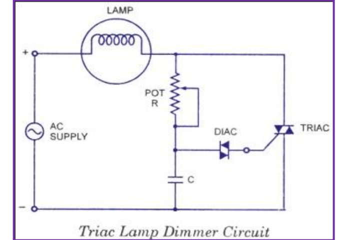


- Notice that the two leads are labelled as terminals T_1 and T_2 instead of the conventional anode-cathode designations. The term DIAC is obtained from capital letters Diode (DI) that can work on AC.
- Conduction occurs in the DIAC when the breakover voltage is reached in either polarity across the two terminals. When T_1 is positive with respect to T_2, and if voltage V_{12} exceeds V_{BO1}, then the structure PNPN conducts. The curve in fig illustrates this characteristic.



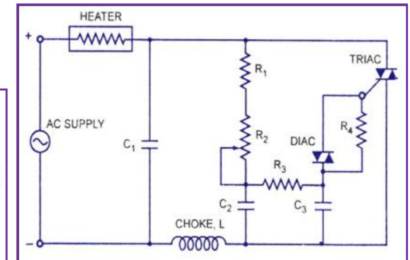
- Similarly, when terminal T_2 is positive with respect T_1 & if voltage V_{21} exceeds breakover voltage V_{B02}, the structure PNPN conducts.
- At voltages less than the breakover voltage, a very small amount current called the leakage current flows through the device.
- Leakage current produced due to the drift of electrons and holes at the depletion region is not sufficient to cause conduction in the device. The device remains practically in non conducting mode.
- This portion of the characteristics shown by region OA in fig is called as the **Blocking State**.
- At point **A**, when the voltage level reaches breakover voltage, the device starts conducting.

- During its conduction, the device exhibits negative resistance characteristics.
- The current flowing in the device starts increasing and the voltage across it starts decreasing.
- This portion of the characteristic shown by AB in Fig. is known as the **Conduction State.**
- The value of current corresponding to the point A is known as the **breakover current.**
- Similar explanation holds good for the negative half-cycle of triggering.
- The characteristic obtained in the third quadrant will be a replica of that obtained in the first quadrant.
- This is because the doping level is same at the two junctions of the device.
- Once the device starts conducting, the current flowing through it is very high which has to be limited by some external resistance.
- In the first quadrant characteristic, T_1 is positive with respective to T_2 whereas in the third quadrant characteristic, T_2 is positive with respect to T_1.
- The value of the breakover voltage for a commonly used DIAC type ST_2 is 30 volts. DIAC is mainly used as a trigger device for TRIAC which require either positive or negative gate pulses to turn ON.



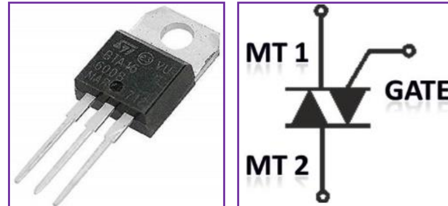
Triac Lamp Dimmer Circuit

- In fact, matched DIAC-TRIAC pairs are available in the market for various types of control circuits.

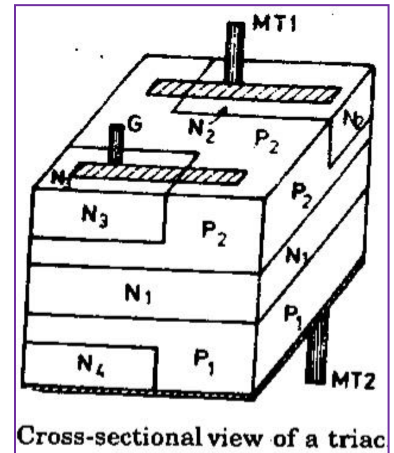


Ψ **Applications of DIAC: -**

- ♣ TRIAC Lamp Dimmer Circuit
- ♣ Heat Control Circuit

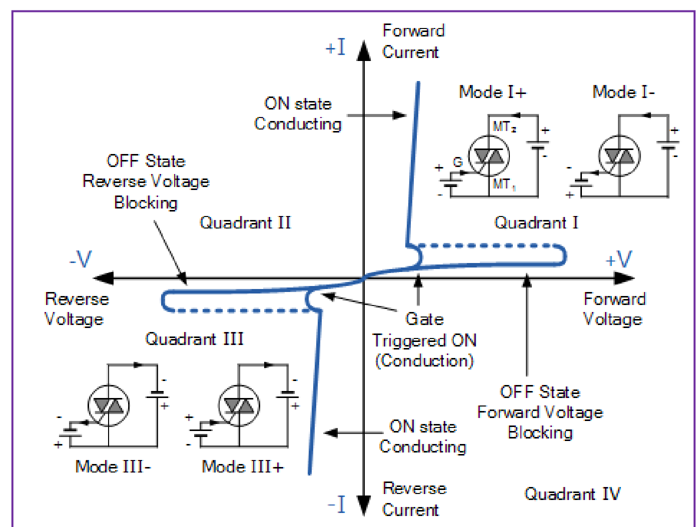


TRIAC



Cross-sectional view of a triac

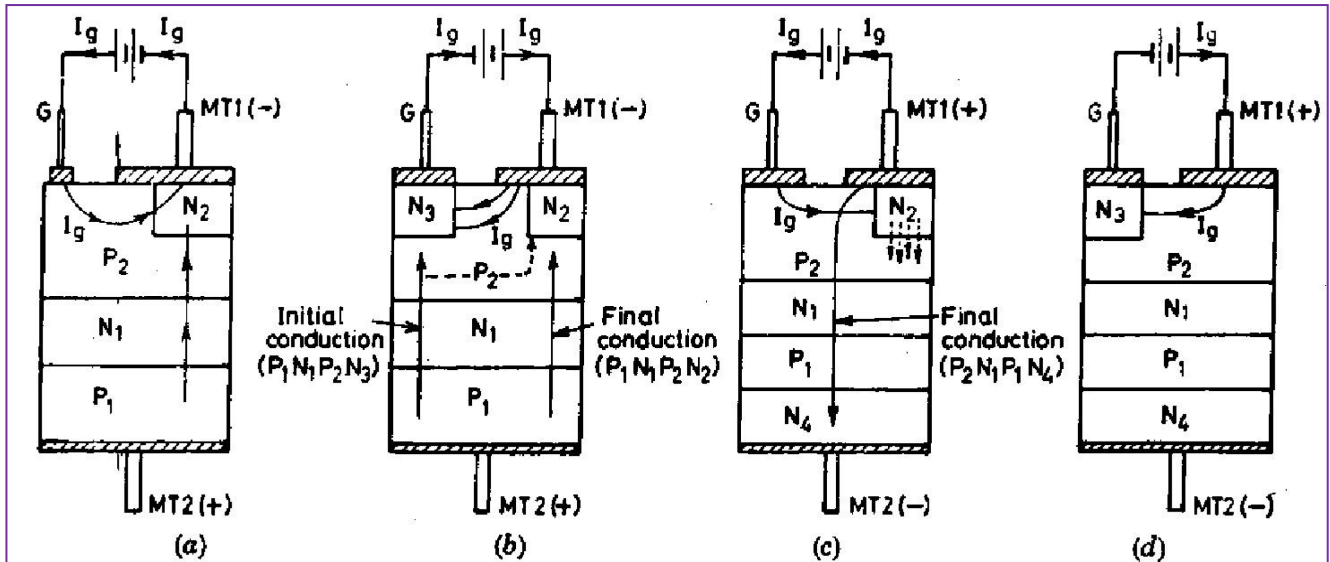
- We have seen that the conventional Thyristor, or SCR, has a reverse-blocking characteristic that prevents current flow in the cathode-to-anode direction. However there are many applications, particularly in a.c. circuits, where bidirectional conduction is required.
- Two thyristors may be connected in inverse-parallel, but at moderate power levels the two anti parallel thyristors can be integrated into a single device structure, as shown in Fig.
- This device, commonly known as Triac (Triode A.C Switch) is represented by the circuit symbol shown in Fig. Triac is the word derived by combining the letters from the word Triode (TRI) and AC.
- As the Triac can conduct in both the direction, the term anode and cathode are not applicable to Triac.
- Its three terminals are usually designated as main terminals MT_1, MT_2 & G, as in Thyristor.
- The terminal MT_1 is the reference point for measurement of voltages and currents at the gate terminal and at the terminal MT_2.
- The gate is near to terminal MT_1.
- The *V-I Characteristic* of TRIAC is in Fig.
- This characteristic of the TRIAC are based on the terminal MT_1 as the reference point.
- The first quadrant is the region in which MT_2 is positive with respect to MT_1 and vice-versa for the third quadrant.



- The peak voltage applied across the device in either direction must be than the breakover voltage in order to retain control by the gate.

- A gate current of specified amplitude of either polarity will trigger the TRIAC into conduction in either quadrant, assuming that the device is in a blocking condition initially before the gate signal is applied.
- The characteristics of a TRIAC are similar to those of an SCR, both in blocking and conducting states, except for the fact that SCR conducts only in the forward direction, where as the TRIAC conduct both the directions.
- Depending upon the polarity of a gate pulse and biasing conditions, the main four layer structure that turns ON by a regenerative process could be one of P_1 N_1 P_2 N_2, P_1 N_1 P_2 N_3 or P_2 N_1 P_1 N_4.

Ψ TRIGGERING MODES OF TRIAC: -



MODES OF OPERATION OF TRIAC

MODE - 1:

- In this mode of operation MT_2 is positive and gate is also positive.
- As MT_2 is positive, so MT_1 should be negative.
- Its connection diagram is shown in side figure.
- When MT_2 is positive with respect to MT_1, junction P_1N_1 and P_2N_2 are forward biased but the junction P_2N_1 is reverse biased.
- When gate terminal is positive with respect to MT_1, gate current flows mainly through P_2N_2 junction like an ordinary SCR as shown in figure.
- When gate current has injected sufficient charge into P_2 layer, reverse biased junction N_1P_2 breaks down as in a normal SCR. Hence TRIAC starts conducting through **P_1N_1 P_2N_2** layer.
- Under this condition TRIAC operates in the first quadrant as shown in figure.
- Under this condition the device is **more sensitive**.

MODE - 2:

- In this mode of operation MT_2 is positive but gate is also negative.
- As MT_2 is positive, so MT_1 should be negative.
- Its connection diagram is shown in side figure.
- When gate terminal is negative with respect to MT_1, gate current flows through P_2N_3 junction and reverse biased junction N_1P_2 is forward biased as in a normal Thyristor.
- As a result, TRIAC starts conducting through P_1N_1 P_2N_3 layer initially as in figure.
- With the condition of **P_1N_1 P_2N_3**, the voltage drop across this path falls but potential or layer between P_2N_3 rises towards the anode potential or MT_2.
- As right hand portion or P_2 is clamped at the cathode potential or MT_1, a potential gradient exist across layer P_2, its left hand region being at higher potential than its right hand region.
- A current shown in dotted is thus established in layer P_2 from left to right.

- This current is similar to conventional gate current is set.
- As a result right hand part of TRIAC consisting main structure.

MODE - 3:

- In this mode of operation MT_2 is negative but gate is also positive.
- As MT_2 is negative, so MT_1 should be positive.
- Its connection diagram is shown in side figure.
- The positive gate current I_g is forward biased P_2N_2 junction.
- Layer N_2 injects electrons into P_2 layer as shown by dotted arrows.
- As a result, reverse biased junction N_1P_1 breaks down as in a conventional Thyristor.
- Eventually the structure **P_2N_1 P_1N_4** is turned on completely.
- Under this condition, the TRIAC operates in third quadrant as shown in figure.

MODE - 4:

- In this mode of operation MT_2 is negative and gate is also negative.
- As MT_2 is negative, so MT_1 should be positive.
- Its connection diagram is shown in side figure.
- When gate terminal is negative with respect to MT_1, gate current flows from P_2 to N_3 and reverse biased junction N_1P_1 is broken like ordinary SCR.
- As a result the structure **P_2N_1 P_1N_4** is turned on completely.
- Under this condition, the TRIAC operates in third quadrant as shown in figure.
- In this mode of operation, the device is **more sensitive**.

POWER TRANSISTORS: -

- Power diodes are uncontrolled devices. In other words, their turn-on and turn-off characteristics are not under control. Power transistors, however, possess controlled characteristics.
- These are turned on when a current signal is given to base, or control, terminal.
- The transistor remains in the on-state so long as control signal is present.
- When this control signal is removed, a power transistor is turned off.
- Power transistors are of four types as under:
  - Bipolar Junction Transistors (BJTs)
  - Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs)
  - Insulated Gate Bipolar Transistors (lGBTs) and
  - Static Induction Transistors (SITs).

Ψ BIPOLAR JUNCTION TRANSISTORS <POWER BJT > : - [*Not Under Your Syllabus]

- A Bipolar Junction Transistor is a three-layer, two junction npn or pnp semiconductor device.
- With one p-region sandwiched by two n-regions, Fig. (a) npn transistor is obtained. With two p-regions sandwiching one n-region, Fig. (b) pnp transistor is obtained.

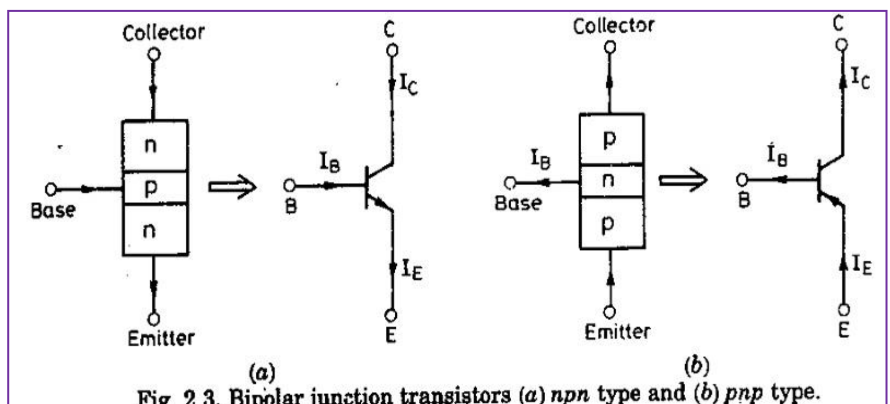
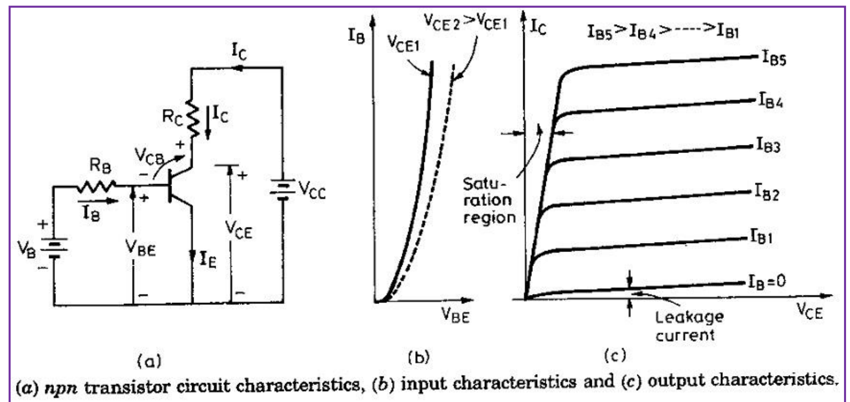


Fig. 2.3. Bipolar junction transistors (a) npn type and (b) pnp type.

- The term 'bipolar' denotes that the current flow in the device is due to the movement of both holes and electrons. A BJT has three terminals named collector (C), emitter (E) and base (B). An emitter is indicated by an arrowhead indicating the direction of emitter current.
- No arrow is associated with base or collector. Power transistors of npn type are easy to manufacture and are cheaper also. Therefore, use of power npn transistors is very wide in high-voltage and high-current applications. Hereafter, npn transistors would only be considered.

Steady-State Characteristics: -



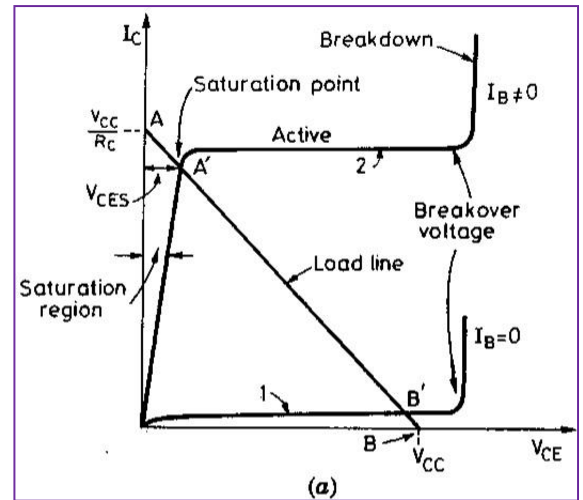
(*a*) *npn* transistor circuit characteristics, (*b*) input characteristics and (*c*) output characteristics.

- Out of the three possible circuit configuration for a transistor, common-emitter arrangement is more common in switching applications.
- So, a common emitter npn circuit for obtaining its characteristics is considered a shown in Fig.

⇨ Input Characteristics: -

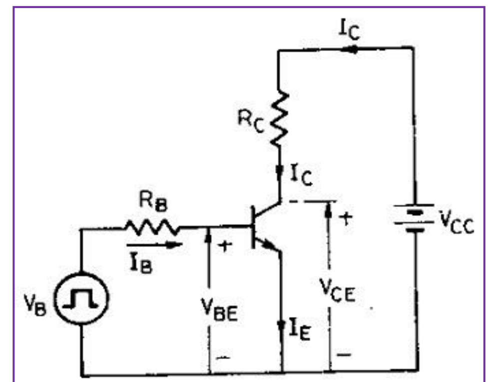
- A graph between base current I_B and base-emitter voltage V_{BE} gives input characteristics.
- As the base emitter junction of a transistor is like a diode, I_B versus V_{BE} graph resembles a diode curve.
- When collector-emitter voltage $V_{CE2} > V_{CE1}$, base current, for the same V_{BE}, decrease as in fig. (b).

⇨ Output Characteristics.



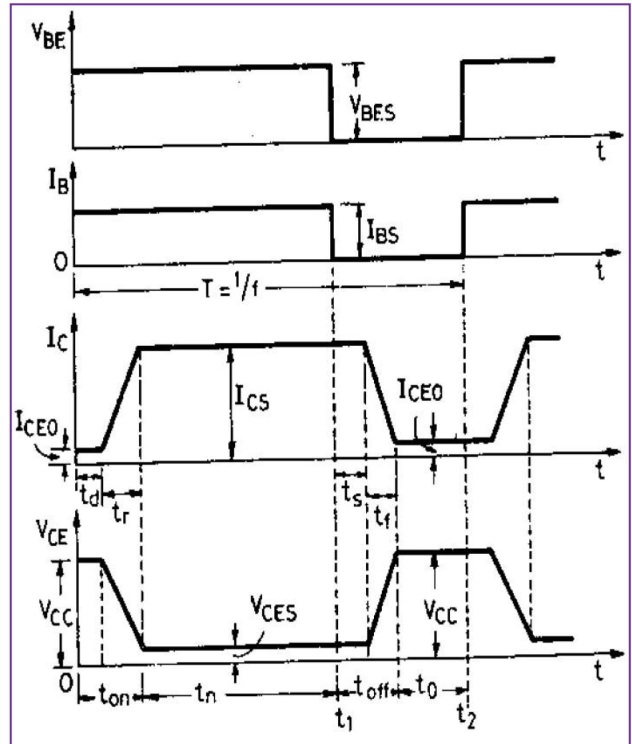
- A graph between collector current I_c and collector-emitter voltage V_{CE} gives output characteristics of a transistor.
- For zero base current. i. e. for $I_B = 0$, as V_{CE} is increased, a small leakage (collector) current exists as shown in fig (c).
- As the base current is increased from $I_B = 0$ to I_{B1}, I_{B2} etc., collector current also rises as in Fig. (c).
- Fig. shows two of the output characteristic curves, 1 for $I_B = 0$ and 2 for $I_B \neq 0$.
- The initial part of curve 2, characterized by low V_{CE} is called the **Saturation Region**.
- In this region he transistor acts like a **switch**. The flat part of curve 2, indicated by increasing V_{CE} and almost constant I_c is the **Active Region**. In this region, transistor acts like an **amplifier**.
- Almost vertically rising curve is the **Breakdown Region** which must be avoided at all costs.
- For load resistor R_C, the collector current I_C is given by $\mathbf{I_C = (V_{CC} - V_{CE}) / R_C}$
- This is the equation of load line. A load line is the locus of all possible operating points.
- Ideally when transistor is ON, $V_{CE} = 0$ and $I_C = V_{CC}/R_C$. This is shown by point A on vertical axis.
- When transistor is OFF or in **Cut-off region**, $V_{CE} = V_{CC}$ and $I_C = 0$. This is shown by point B.
- For resistive load, the line joining points A & B is the load line.

BJT Switching Performance: -



- When base current is applied, a transistor does not turn on instantly because of the presence of internal capacitances.
- Fig. shows the various switching waveforms of an *npn* power transistor with resistive load between collector & emitter.
- When input voltage V_B to base circuit is made $-V_2$ at t_o, junction EB or EBJ is reverse biased, $v_{BE} = -V_2$, the transistor is off, $i_B = I_C = 0$ and $v_{CE} = V_{cc}$.
- At time t_1 input voltage v_B is made $+V_1$ and i_B rises to I_{B1}. After t_1, base-emitter voltage v_{BE} begins to rise gradually from $-V_2$ and collector current i_c begins to rise from zero (actually a small leakage current I_{CEO} exists) & collector-emitter voltage V_{CE} starts falling from its initial value V_{CC}.
- After some time delay t_d, called delay time, the collector current rises to $0.1I_{CS}$, v_{CE} falls from V_{CC} to $0.9 V_{CC}$ and v_{BE} reaches $V_{BES} = 0.7$ V.

- This delay time is required to charge the base-emitter capacitance to $V_{BES} = 0.7$ V.
- Thus, **delay time** (t_d) is defined as the time during which the collector current rises from zero to $0.1I_{CS}$ & collector-emitter voltage falls from V_{CC} to $0.9\ V_{CC}$.
- After delay time t_d, collector current rises from $0.1I_{CS}$ to $0.9I_{CS}$ & v_{CE} falls from $0.9\ V_{CC}$ to $0.1\ V_{CC}$ in time t.
- This time t is known as rise time which depends upon transistor junction capacitances.
- **Rise Time** (t_r) is defined as the time during which collector current rises from $0.1\ I_{CS}$ to $0.9\ I_{CS}$ and collector-emitter voltage falls from $0.9\ V_{CC} \rightarrow 0.1\ V_{CC}$.
- This shows that **total turn-on time**, $t_{on} = t_d + t_r$.
- Value of ton is of the order of 30 to 300 nano seconds.
- The transistor remains in the on or saturated state so long as input voltage stays at V_1.
- In case transistor is to be turned off, then input voltage v_B and input base current i_B are reversed.
- At time t_2, input voltage v_B to base circuit is reversed from V_1 to $- V_2$.



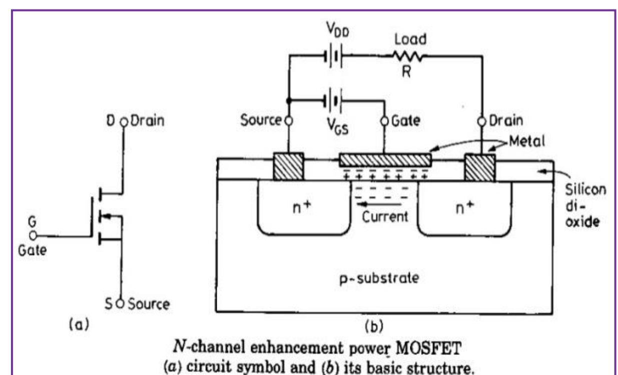
- At the same time, base current changes from I_{B1} to $- I_{B2}$ as shown in Fig.
- Negative base current I_{B2} removes excess carriers from the base. The time t_s required to remove these excess carriers is called storage time and only after t_s base current I_{B2} begins to decrease towards zero.
- Transistor comes out of saturation only after t_s. **Storage Time** (t_s) is defined as the time during which collector current falls from I_{CS} to $0.9\ I_{CS}$ & collector emitter voltage V_{CE} rises from V_{CES} to $0.1\ V_{CC}$.
- Negative input voltage enhances the process of removal of excess carriers from base and hence reduces the storage time and therefore, the turn-off time.
- After t_s collector current begins to fall and collector-emitter voltage starts building up.
- **Fall Time** (t_f) is defined as the time during which collector current drops from $0.9\ I_{CS}$ to $0.1\ I_{CS}$ and collector emitter voltage V_{CE} rises from $0.1\ V_{CC}$ to $0.9\ V_{CC}$. The Sum of storage time and fall time gives the transistor **Turn-Off Time** (t_{off}) i.e. $t_{off} = t_s + t_f$.

Applications of BJT in Power switching applications:-

- The applications of BJT are Switching and Amplification.
- For switching applications transistor is biased to operate in the saturation or cutoff region.
- Transistor in cutoff region will act as an open switching and in saturation will act as a closed switch.

POWER MOSFET: -

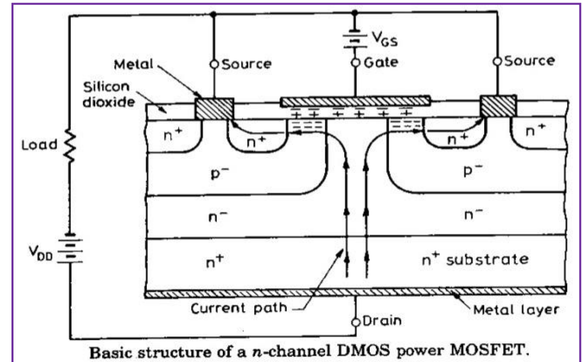
- A Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is a recent device developed by combining the areas of Field-Effect concept & MOS technology.
- A power MOSFET has three terminals called drain (D), source (S) and gate (G) in place of the corresponding three terminals Collector, Emitter and Base for BJT.
- The circuit symbol of Power MOSFET is shown in Fig.
- Arrow indicates the direction of electron flow.



N-channel enhancement power MOSFET
(*a*) circuit symbol and (*b*) its basic structure.

- A BJT is a current controlled device whereas a power MOSFET is a voltage controlled device.
- As its operation depends upon the flow of majority carriers only, MOSFET is a unipolar device.
- The control signal, or base current in BJT is much larger than required in a MOSFET.
- This is due to the fact that gate circuit impedance in MOSFET is extremely high, of the order of $10^9\ \Omega$.

- This large impedance permits the MOSFET gate to be driven directly from microelectronic circuits.
- BJT suffers from second breakdown voltage whereas MOSFET is free from this problem.
- Power MOSFETs are now finding increasing applications in low-power high frequency converters.
- Power MOSFETs are of **two** types**:** ~ n - channel and p - channel enhancement MOSFET.
- Out of these two types, n-channel enhancement MOSFET is more common because of higher mobility of electrons. As such, only this type of MOSFET is studied in what follows.
- A simplified structure of n-channel planar MOSFET of low power rating is shown in Fig. (b).
- On p-substrate (or body), two heavily doped n^+ regions are diffused as shown. An insulating layer of silicon dioxide (SiO_2) is grown on the surface.
- Now this insulating layer is etched in order to embed metallic source and drain terminals.
- Note that n^+ regions make contact with source and drain terminals as shown. A layer of metal is also deposited on SiO_2 layer so as to form the gate of MOSFET in between source and drain terminals.

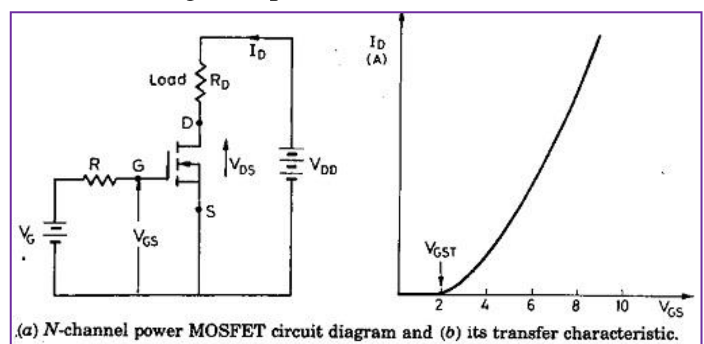


Basic structure of a *n*-channel DMOS power MOSFET.

- When gate circuit is open, junction between n^+ region below drain and p-substrate is reverse biased by input voltage V_{DD}. Therefore, no current flows from drain to source and load.
- When gate is made positive with respect to source, an electric field is established as shown in Fig. (b).
- Eventually, induced negative charges in the p-substrate below SiO_2 layer are formed thus causing the p layer below gate to become an induced n layer. These negative charges, called electrons, form n-channel between two n^+ regions and current can flow from drain to source as shown by the arrow.
- If V_{GS} is made more +ve, induced n - channel becomes more deep so more current flows from D to S.
- This shows that drain current I_D is enhanced by the gradual increase of gate voltage, hence the name enhancement MOSFET.
- The main **disadvantage** of n-channel planar MOSFET is that conducting n-channel in between drain and source gives large on-state resistance. This leads to high power dissipation in n-channel.
- This shows that planar MOSFET construction of Fig. (b) is feasible only for low-power MOSFETs.
- The constructional details of high power MOSFET is shown in Fig.
- In this figure is shown a planar Vertical Diffused Metal Oxide semiconductor (VDMOS) structure for n^- channel which is quite common for power MOSFETs.
- On n^+ substrate, high resistivity n^- layer is epitaxially grown.
- The thickness of n^- layer determines voltage blocking capability of the device.
- On the other side of n^+ substrate, a metal layer is deposited to form the drain terminal.
- Now p region are diffused in the epitaxially grown n^- layer.
- Further, n^+ regions are diffused in p regions as shown. As before, SiO_2 layer is added, which is then etched so as to fit metallic source and gate terminals. A power MOSFET actually consists of parallel connection of thousands of basic MOSFET cells on the same single chip of silicon.

Ψ PMOSFET Characteristics: -

- The static characteristics of power MOSFET are now described briefly. The basic circuit diagram for n-channel PMOSFET is shown in Fig.
- Where voltages and currents are as indicated. The source S is taken as common terminal, as usual, between the input and output of a MOSFET.

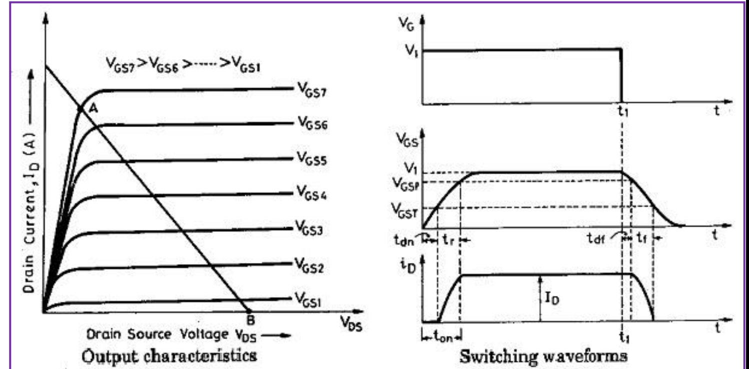


(a) *N*-channel power MOSFET circuit diagram and (b) its transfer characteristic.

(a) **Transfer Characteristics: -**

- This characteristic shows the variation of drain current I_D as a function of gate-source voltage V_{GS}.
- Fig. (b) shows typical transfer characteristics for n-channel PMOSFET.
- Threshold voltage V_{GST} is an important parameter of MOSFET.
- V_{GST} is the minimum positive voltage between gate and source to induce n-channel. Thus, for threshold voltage below V_{GST}, device is in the off-state. Magnitude of V_{GST} is of the order of 2 to 3V.

(b) **Output Characteristics: -**



- PMOSFET output characteristics, shown in Fig. (a), indicate the variation of drain current I_D as a function of Drain-Source voltage V_{DS} with Gate-Source voltage V_{GS} as a parameter.
- For low values of V_{DS}, the graph between I_D-V_{DS} is almost linear; this indicates a constant value of on-resistance $R_{DS}=V_{DS}/I_D$.
- For given V_{GS}, if V_{DS} is increased, output characteristic is relatively flat, indicating that drain current is nearly constant.
- A load line intersects the output characteristics at A and B. Here A indicates fully-on condition and B fully-off state. PMOSFET operates as a switch either at A or at B just like a BJT.
- When power MOSFET is driven with large gate- source voltage, MOSFET is turned on, $V_{DS.ON}$ is small.
- Here, the MOSFET acting as a closed switch is said to be driven into ohmic region (called saturation region in BJT). When device turns on, PMOSFET traverses i_D – V_{DS} characteristics from cut-off, to active region and then to the ohmic region.
- When PMOSFET turns off, it takes backward journey from ohmic region to cutoff state.

SN	Power BJT	Power MOSFET
1.	BJT is a minority as well as majority carrier device	MOSFET is majority carrier device
2.	BJT is Current Controlled Device	MOSFET is Voltage Controlled Device
3.	BJT has a negative temperature coefficient.	BJT has a positive temperature coefficient
4.	It can't operate at very high frequency.	It can operate at very high frequency.
5.	It is less sensitive to voltage spike.	It is more sensitive to voltage spike.
6.	The on-state voltage is low, So on-state loss is low.	The on-state voltage is hig, So on-state loss is higher than BJT.
7.	Conduction losses are less.	Conduction losses are higher.
8.	Switching losses are more.	Switching losses are less.
9.	More energy efficient at low frequency.	More energy efficient at High frequency.

(c) **Switching Characteristics: -**

- The switching characteristics of a power MOSFET are influenced to a large extent by the internal capacitance of the device & internal impedance of the gate drive circuit.
- At turn-on there an initial delay t_{dn} during which input capacitance charges to gate threshold voltage V_{GST}.
- Here t_{dn} is called **Turn-On Delay Time**.
- There is further delay t_r, called rise time, during which gate voltage rises to V_{GSP}, a voltage sufficient to drive the MOSFET into ON state. During t_r, drain current rises from zero to full-on current I_D.
- Thus, the Total Turn-ON Time is $t_{on} = t_{dn} + t_r$.
- The turn-on time can be reduced by using low-impedance gate-drive source.
- As MOSFET is a majority carrier device, turn-off process is initiated soon after removal of gate voltage at time t_1. The **Turn-Off Delay Time** (t_{df}) is the time during which input capacitance discharges from overdrive gate voltage V_1 to V_{GSP}. Thus, the Total Turn-OFF Time is $t_{off} = t_{df} + t_f$.
- The fall time, t_f, is the time during which input capacitance discharges from V_{GSP} to threshold voltage.
- During t_f, drain current falls from I_D to zero. So when $V_{GS} \le V_{GST}$, PMOSFET turn-off is complete.

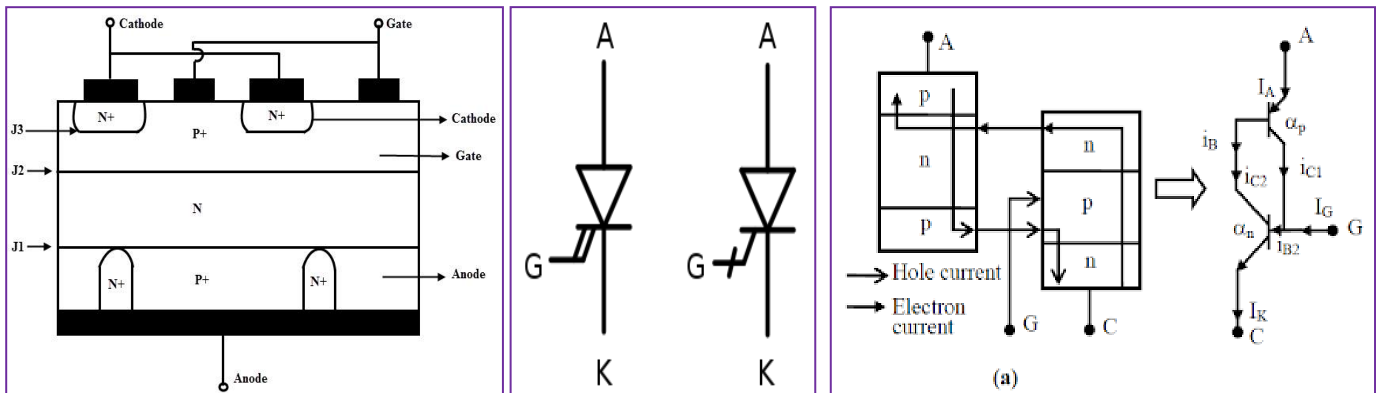
Ψ **PMOSFET Applications: -**

- The on-resistance of MOSFET increases with voltage rating; this makes the device very lossy at high-current applications.
- Since the on-resistance has positive temperature coefficient, parallel operation of PMOSFETs is easy.

- The positive temperature coefficient also reduces the second breakdown effect in PMOSFETs.
- PMOSFETs find applications in high-frequency switching applications, varying from a few watts-kWs.
- The device is very popular in switched-mode power supplies and inverters.
- These are, at present available with 500 V, 140 A ratings.

GTO <GATE TURN OFF THYRISTOR>: -

- Conventional Thyristors (CTs) are nearly ideal switches for their use in power electronics applications.
- These can easily be turned on by positive gate current. Once in the on state, gate loses control.
- CTs can now be turned off by expensive and bulky commutation circuitry.
- This shortcoming of thyristors limits their use upto about 1 kHz application.
- These drawbacks in thyristors have led to the development of GTOs.
- It is more versatile power-semiconductor device. It is like a CT but with added features in it.
- A GTO can easily be turned off by a negative gate pulse of appropriate amplitude.
- Thus, a GTO is a **pn pn** device that can be turned-on by a positive gale current and turned-off by a negative gate current at its gate cathode terminals.
- Self-turn off capability of GTO makes it the most suitable device for inverter chopper applications.



Ψ Basic Structure: -

- A GTO is pn pn, three terminal device with anode (A), cathode (K) and gate (G) as in fig (1).
- The four layers are **p^+ n p^+ n^+** as shown. In CT, anode consists of p^+ layer, but in a GTO anode is made up of n^+ type fingers diffused into p^+ layer. Two alternate circuit symbols for GTO are shown in Fig (2).
- Since GTO is a four layer pn pn device just like CT, it can also be modelled by Two-Transistor Analogy as shown in fig (3). The four layers have different doping levels indicated by p^+ n p^+ n^+.
- Transistor Q_1 is p^+ n p^+ type and transistor Q_2 is n p^+ n^+, with p^+ emitter of Q_1 as anode A and n^+ o emitter of Q_2 as cathode K.

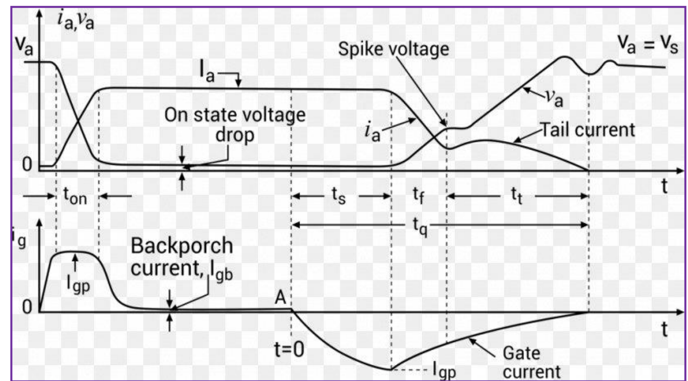
Ψ Static V-I Characteristics: -

- The static V-I characteristics of a GTO is **identical with that of a conventional Thyristor**.
- Latching current for GTO is however several amperes, say 2A, as compared to 100-500 mA for CT of the same rating. If gate current is not able to turn on GTO, it behaves like a high-voltage, low gain transistor with considerable anode current. This leads to a noticeable power loss under such conditions.
- In reverse mode, reverse-voltage blocking capability of GTO is low, typically 20 to 30V, because of (i) anode shorts and (ii) large doping densities on both sides of reverse blocking junction J_3.

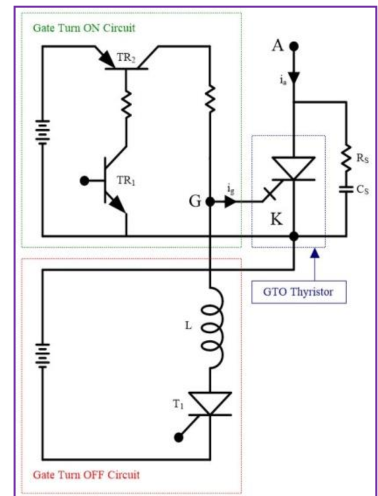
Ψ Dynamic or Switching Characteristics: -

- The basic gate drive circuit for a GTO is shown in Fig next page. For turning-on a GTO, first transistor TR_1 is turned on, this in turn switches on TR_2 to apply a positive gate-current pulse to turn on GTO.
- For turning off the GTO, the turn-off circuit should be capable of outputting a high peak current.
- Usually, a thyristor is used for this purpose. In Fig. turn-off process is initiated by gating thyristor T_1.
- When T_1 is turned on, a large negative gate current pulse turns off the GTO.

♣ Gate Turn – On: -



- The turn-on process in a GTO is similar to a CT.
- Gate turn-on time for GTO is made up of delay time, rise time & spread time like a CT.
- Further, turn-on time in a GTO can be decreased by increasing its forward gate current like SCR.
- In fig, a steep-fronted gate pulse is applied to turn-on GTO. Gate drive can be removed once anode current exceed latching current.
- However, some manufacturers advise that even after GTO is on, a continuous gate current, called *back porch current,* I_{gb} as shown, should be applied during the entire on-period of GTO.
- The aim of this recommendation is to avoid any possibility of unwanted turn-off of the GTO.



♣ Gate Turn – Off: -

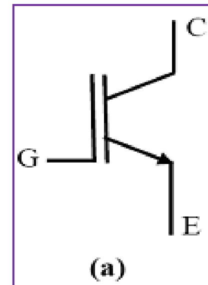
- The turn-off characteristics of a GTO are different from an SCR.
- Before the initiation of turn-off process, a GTO carries a steady current I_a.
- This fig shows a typical dynamic turn-off characteristic for a GTO.
- The **Total Turn-off Time** (t_q) is subdivided into three different periods; namely the **Storage Period** (t_s), **Fall Period** (t_f) and **Tail Period** (t_t).
- In other words, $\mathbf{t_q = t_s + t_f + t_t}$.
- Initiation of turn-off process starts as soon as negative gate current begin to flow after t = 0 at instant A.
- The rate of rise of this gate current depends upon the gate circuit inductance L & gate voltage applied.
- During the storage period, anode current $\mathbf{I_a}$ & anode voltage (on-state voltage drop) remain constant.
- Termination of the storage period is indicated by a fall in $\mathbf{I_a}$ and rise in $\mathbf{V_a}$.
- During $\mathbf{t_s}$ excess charges, i.e. hole, in $\mathbf{p^+}$ base are removed by negative gate current and the centre junction comes out of saturation.
- In other words, during storage time $\mathbf{t_s}$, the negative gate current rises to a particular value and prepare the GTO for turning-off (or commutation) by flushing out the stored earn carriers.
- After $\mathbf{t_s}$**,** anode current begins to fall rapidly and anode voltage starts rising. As shown in fig, the anode current falls to a certain value and then abruptly changes its rate of fall.
- This interval during which anode current falls rapidly is the fall time $\mathbf{t_f}$, and is order of 1 μs.
- The fall period $\mathbf{t_f}$ is measured from the instant gate current is maximum to the instant anode current falls to its tail current. At the time $\mathbf{t = t_s + t_f}$, there is a spike in voltage due to abrupt change in anode current.
- Then anode current & voltage keep moving towards their turn-off value for a time $\mathbf{t_t}$ called **tail time**.
- After $\mathbf{t_t}$, anode current reaches zero value and v_a undergoes a transient overshoot due to the presence of R_s, C_s and then stabilized to its off-state value equal to the source voltage applied to the anode circuit.
- Here R_s and C_s are the snubber circuit parameters. The turn-off process is complete when tail current reaches zero. The overshoot voltage and tail current can be decreased by increasing the size of C_s, but a compromise with snubber loss must be made. The duration of t_t depends upon the device characteristics.

Ψ Application of GTOs: -

- GTOs are used in variable speed motor drives, high power inverters, static VAR compensators (SVCs) and AC/DC power supplies with high power ratings and traction. Also used in high-performance drive such as the field-oriented control scheme used in rolling mills, robotics and machine tools.

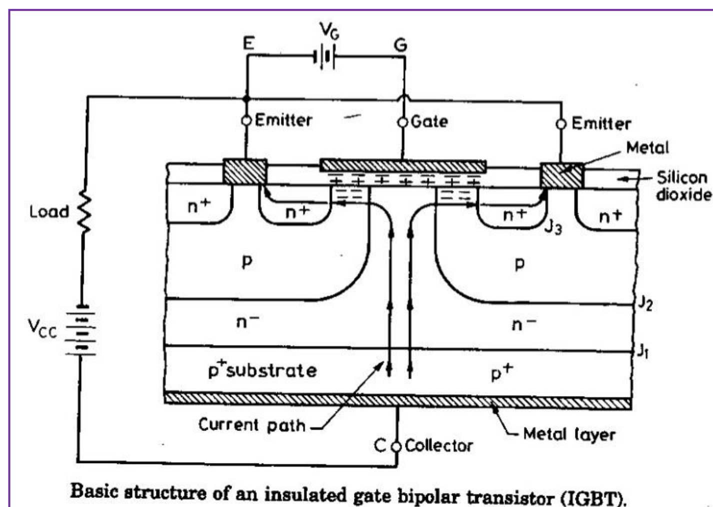
IGBT <Insulated Gate Bipolar Transistor>: -

- IGBT has been developed by combining into it the best qualities of both BJT and PMOSFET.



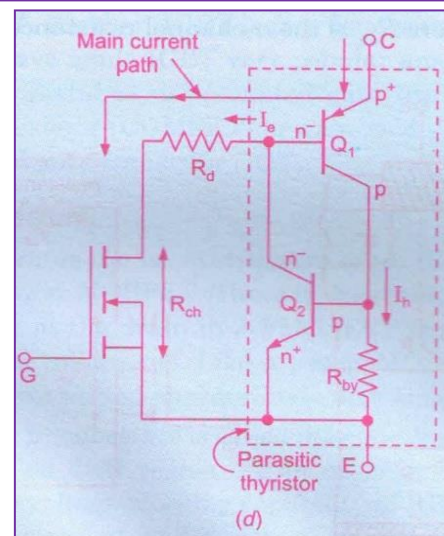
- Thus IGBT process high input Impedance like a PMOSFET and has low on-state power loss like BJT. It is free from second breakdown problem like in BJT.
- All these merits have made IGBT very popular amongst power-electronics engineers.
- IGBT is also known as Metal Oxide Insulated Gate Transistor (**MOSIGT**), Conductively-Modulated Field Effect Transistor (**COMFET**) or Gain-Modulated FET (**GEMFET**). It was also initially called Insulated Gate Transistor (**IGT**).

Ψ Basic Structure



Basic structure of an insulated gate bipolar transistor (IGBT).

- Fig illustrates the basic structure of an IGBT.
- It is constructed virtually in the same in the same manner as a Power MOSFET.
- There is a major difference in the substrate.
- The n^+ layer substrate at the drain in a PMOSFET is now substituted in the IGBT by p^+ layer substrate called collector C.
- Like PMOSFET, an IGBT has also thousands of basic structure cells connected appropriately on a single chip of silicon.
- In IGBT, p^+ substrate is called **injection layer** because it injects holes into n^- layer.
- The n^- layer is called **drift region**.
- As in semiconductor devices, thickness of n^- layer determines the voltage blocking capability of IGBT.
- The p layer is called body of IGBT. The n^- layer in between p^+ region and p region serves to accommodate the depletion layer of pn^- junction, i.e. junction J_2.



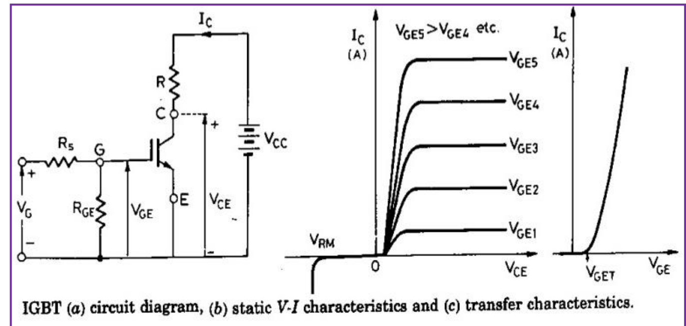
Ψ Working: -

- When collector is made positive with respect to emitter, IGBT gets forward biased. With no voltage between gate and emitter, two junctions between n^- region and p region (J_2) are reverse biased; so no current flows from collector to emitter as shown in fig.
- When gate is made positive with respect to emitter by voltage V_G, with gate-emitter voltage more than the threshold voltage V_{GET} of IGBT, an n-channel or inversion layer, is formed in upper part of p region just beneath the gate, as in PMOSFET. This n-channel short-circuits the n^- region with n^+ emitter regions.
- Electrons from the n^+ emitter begin to flow to n^- drift region through n-channel. As IGBT is forward biased with collector positive and emitter negative, p^+ collector region injects holes into n^- drift region.
- In short, n^- drift region is flooded with electrons from p-body region and holes from p^+ collector region.
- With this, the injection carrier density in n^- drift region increases considerably and as a result, conductivity of n^- region enhances significantly. Therefore, IGBT gets turned on and begins to conduct forward current I_C. Collector current I_C or emitter current I_E consists of two current components: -
- (i) Hole current I_h due to injected holes flowing from collector, $p^+ n^- p$ transistor Q_1, p-body region resistance R_{by} and emitter. (ii) Electronic current I_e due to injected electrons flowing from collector, injection layer p^+, drift region n^-, n-channel resistance R_{ch}, n^+ and emitter.
- This means that collector, or load, current I_C = emitter current $I_E = I_h + I_e$. Major component of collector current is electronic current I_e, Thus $I_C \approx I_E$. Main current path for collector, or load, current is through p^+, n^-, drift resistance R_d and n-channel resistance R_{ch} as shown in Fig.

- Therefore, the voltage drop in IGBT in its on-state is $\mathbf{V_{CE.ON} = I_C . R_{ch} + I_C . R_d + V_{jl}}$
 = Voltage drop [in n-channel + across drift in n^- region + across forward biased $p^+ n^-$ junction J_l]
- Here V_{J1} is usually 0.7 to 1 V as in a p-n diode. The voltage drop $I_C.R_{ch}$ is due to n-channel resistance, almost the same as in a PMOSFET.
- The voltage drop $V_{df} = I_C.R_d$ in IGBT much less than that in PMOSFET. It is due to substantial increase in the conductivity caused by injection of electrons and holes in n^- drift region.
- Conductivity enhancement is the main reason for low on-state voltage drop in IGBT than PMOSFET.

Ψ <u>IGBT Characteristics</u>: -

- The circuit of Fig. (a) shows the various parameters pertaining to IGBT characteristics.
- Static I-V or **Output Characteristics** of an IGBT (n-channel type) show the plot of collector current I_C versus collector-emitter voltage V_{CE} for various values of gate-emitter voltages V_{GE1}, V_{GE2} etc.
- These characteristics are shown in Fig. (b).

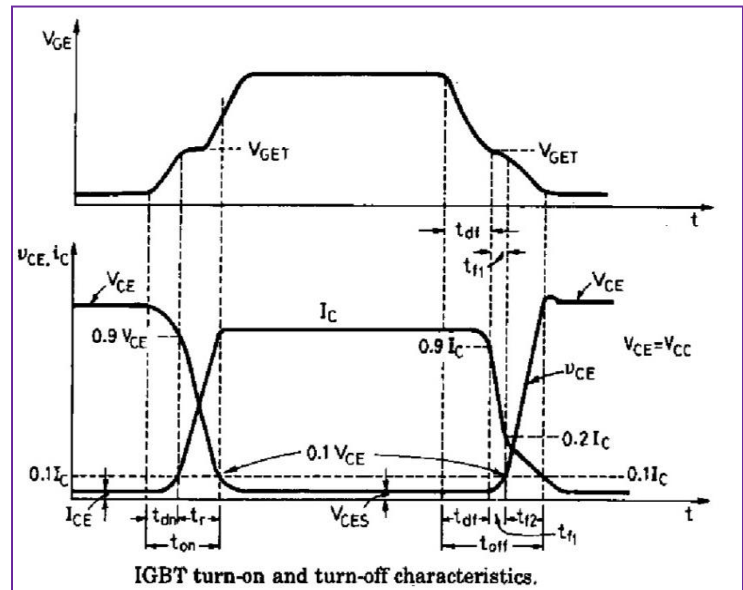


IGBT (a) circuit diagram, (b) static V-I characteristics and (c) transfer characteristics.

- In the forward direction, the shape of the output characteristics is similar to that of BJT. But here the controlling parameter is gate-emitter voltage V_{CE} because IGBT is a voltage-controlled device.
- When the device is off, junction J_2 blocks forward voltage and in case reverse voltage appears across collector and emitter, junction J_1 blocks it. In Fig. (b), V_{RM} is the maximum reverse breakdown voltage.
- The **Transfer Characteristic** of an IGBT is a plot of Collector Current I_C verses Gate Emitter voltage V_{GE} as shown in Fig (c). This characteristic is identical to that of power MOSFET.
- When V_{GE} is less than the threshold voltage V_{GET}, IGBT is in the off-state.

Ψ <u>Switching Characteristic</u>: -

- The Switching characteristic of the IGBT →
- The turn-on time is defined as the time between the instants of forward blocking to forward on-state.
- Turn-on is composed of delay time $\boldsymbol{t_{dn}}$ and rise time $\boldsymbol{t_r}$. i.e. $\boldsymbol{t_{on} = t_{dn} + t_r}$.
- Delay time is defined as the time for collector emitter voltage fall from V_{CE} to $0.9V_{CE}$.
- Here V_{CE} is the initial collector emitter voltage. Time $\boldsymbol{t_{dn}}$ may also be defined as the time for the collector current to rise from its initial leakage current I_{CE} to 0.1 I_C.
- Here I_C is the final value of collector current.



IGBT turn-on and turn-off characteristics.

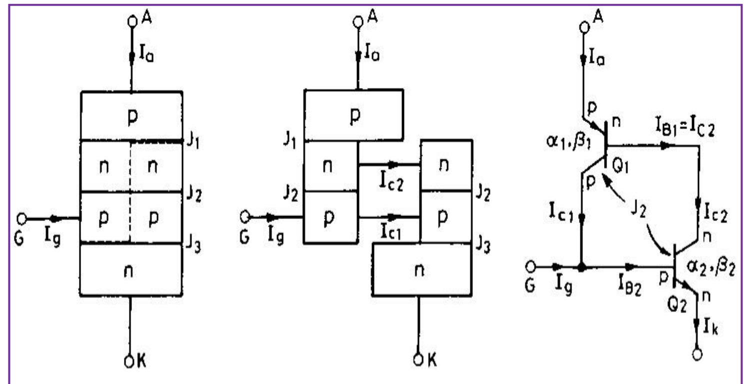
- The **rise time** t_r is the time during which collector-emitter voltage falls from 0.9 V_{CE} to 0.1 V_{CE}.
- It is also defined as the time for the collector current to rise from 0.1 I_C to its final value I_C.
- After time $\boldsymbol{t_{on}}$ the collector current I_C and the collector-emitter voltage falls to small value called **conduction drop** = V_{CES} where subscript S denotes saturated value.
- The turn-off time is somewhat complex. It consists of three time intervals: (**i**) Delay Time, (t_{df}) (**ii**) Initial Fall Time, (t_{f1}) and (**iii**) Final Fall Time (t_{f2}); i.e. $\boldsymbol{t_{off} = t_{df} + t_{f1} + t_{f2}}$
- The delay time is the time during which gate voltage falls from V_{GE} to threshold voltage V_{GET}.
- As V_{GE} falls to V_{GET} during t_{df}, the collector current falls from I_C to 0.9 I_C.
- At the end of t_{df}, collector-emitter voltage begins to rise.

- The first fall time t_{f1} is defined as the time during which collector current falls from 90 to 20% of its initial value I_C, or the time during which collector-emitter voltage rises from V_{CES} to 0.1 V_{CES}.
- The final fall time t_{f2} is the time during which collector current falls from 20 to 10% of I_C, or the time during which collector-emitter voltage rises from 0.1 V_{CE} to final value V_{CE} as shown in figure.

Ψ Applications of IGBT: -IGBTs are used in high power applications such as:

- ♣ Appliance motor drives
- ♣ Electric vehicle motor drives
- ♣ Power factor correction converters
- ♣ Uninterruptible power supplies
- ♣ Solar inverters
- ♣ High frequency welders
- ♣ Inductive heating cookers

Ψ The Two Transistor Analogy of SCR: -



- The operation of an SCR can also be explained in a very simple way by considering it in terms of two transistors. This is known as the Two Transistor Analogy of SCR.
- The SCR can be considered as an npn and a pnp transistor, where the collector of one transistor is attached to the base of the other and vice versa, as shown in Fig.
- This model is obtained by splitting the two middle layers of the SCR into two separate parts.
- It is observed from the figure that the collector current of transistor T_1 becomes the base current of transistor T_2 and vice versa. Thus, $I_{c1} = I_{b2}$ & $I_{b1} = I_{c2}$ Also $I_k = I_a + I_g$ --- (1)
- We have the relation from transistor analysis, $I_{bl} = I_{e1} - I_{c1}$--- (2) Also, $I_{c1} = \alpha_l I_{e1} + I_{co1}$ --- (3)
- Where I_{co1} is the reverse leakage current of the reverse biased junction J_2 when the two outer layers are not present. Substituting Eq. (3) in Eq. (2) we get $I_{bl} = I_{e1} - \alpha_l I_{e1} - I_{co1} = (1 - \alpha_l) I_{e1} - I_{co1}$ ---------- (4)
- From Fig. it is evident that the anode current of the device becomes the emitter current of transistor T_1 that is $I_a = I_{e1}$. Thus the Eq. (4) becomes $I_{bl} = (1 - \alpha_l) I_a - I_{co1}$----- (5)
- Also $I_{c2} = \alpha_2 I_{e2} + I_{co2}$. So from Fig it is observed that the cathode current of the SCR becomes the emitter current of transistor T_2 that is $I_k = I_{e2}$. Thus $I_{c2} = \alpha_2 I_k + I_{co2}$ ----- (6). But $I_{b1} = I_{c2}$ ---- (7)
- Now substituting Eq. (5) & (6) in Eq. (7), we get $(1 - \alpha_l) I_a - I_{co1} = \alpha_2 I_k + I_{co2}$ ---- (8)
- Now substituting Eq. (1) in Eq. (8), we get $(1 - \alpha_l) I_a - I_{co1} = \alpha_2 (I_a + I_g) + I_{co2}$
  - ⇨ $(1 - \alpha_l) I_a - I_{co1} = \alpha_2 (I_a + I_g) + I_{co2}$ ➔ $I_a - \alpha_l I_a - \alpha_2 I_a = \alpha_2 I_g + I_{co2} + I_{co1}$
  - ⇨ $(1 - \alpha_l - \alpha_2) I_a = \alpha_2 I_g + I_{co2} + I_{co1}$ ➔ $[1 - (\alpha_l + \alpha_2)] I_a = \alpha_2 I_g + I_{co2} + I_{co1}$
  - ⇨ Thus $$I_a = \frac{\alpha_2 I_g + I_{co2} + I_{co1}}{[1 - (\alpha_1 + \alpha_2)]}$$ ------- (9)
- Assuming the leakage current of transistor T_1 & T_2 to be negligible small, $$I_a = \frac{\alpha_2 I_g}{[1 - (\alpha_1 + \alpha_2)]}$$ --- (10)
- From Eq. (10), it can be analyzed that if $(\alpha_l + \alpha_2) = 1$, the value of anode current I_a becomes infinite, that is, the anode current suddenly attains a very high value, approaching infinity.
- In other words, we can say that the device suddenly latches into conduction (ON) state from the non-conduction (OFF) state. This characteristic of the device is known as its **regenerative action**.
- This can also be stated the gate current I_g is of such a value that $(\alpha_l + \alpha_2)$ approaches unity value, device will trigger. This turn-on condition $\{(\alpha_l + \alpha_2) \geq 1\}$ of SCR can be satisfied in the following ways: -
  - ♣ If the temperature of the device is very high, the leakage current through it increases, which may then satisfy the required condition to turn it on.
  - ♣ When the current through the device is extremely small, the alphas will be very small and the condition for breakover can be satisfied only by large values of holes multiplication factor M_p and electron multiplication factor M_n.

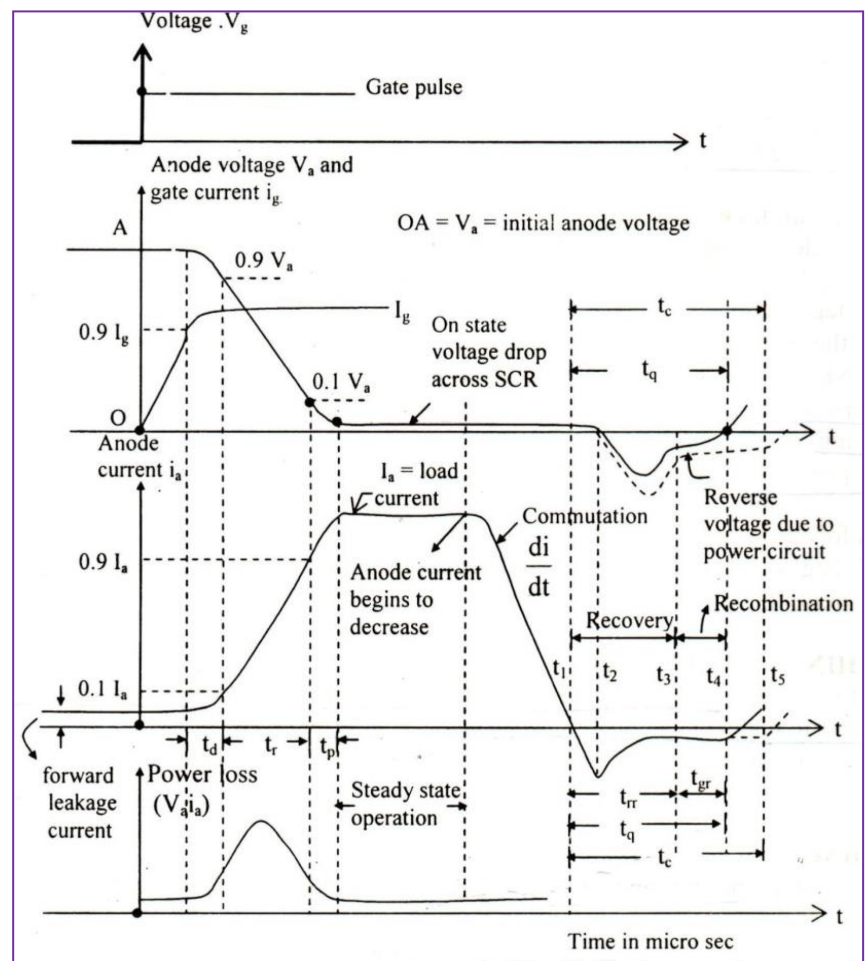
- ♣ Near the breakdown voltage of junction J_2, the multiplication factors are very high and the required condition for breakover can be obtained by increasing the voltage across the device to V_{BO}, which will close the breakdown voltage of junction J_2.
- ♣ The required condition for breakover can also be realized by increasing α_l and α_2. In Fig if a current I_g is injected into the base P in the same direction as current I_a across J_2, the current gain of the NPN transistor can now be increased independently of the anode to cathode voltage V_a and current I_a because α_2 depends on $(I_a + I_g)$ and α_l would still, depend on I_a.
- ♣ The total current gain will now depend on I_g and independent means of breakover is obtained. The presence of gate current modifies the static V-I characteristics as shown in fig.

Ψ **Dynamic TURN-ON Switching Characteristics of SCR: -**

- ➢ The static characteristic gives no indication as to the speed at which the SCR is capable of being switched from the forward blocking voltage to the conducting state and vice-versa.
- ➢ However, the transition from one state to the other does not take place instantaneously; it takes a finite period of time. This is illustrated in Fig. as shown the total turn-on time t_{on} of the SCR is subdivided into three distinct periods, called the **Delay Time**, **Rise Time** and **Spread Time**.
- ➢ These time periods are defined in terms of the waveforms of the anode voltage and current obtained in a circuit in which the anode-load consists of a pure-resistance.

♣ **Delay Time (t_d): -**

- ➢ This is the time between the instant at which the gate current reaches 90% of its final value and the instant at which the anode current reaches 10% of its final value.
- ➢ It can also be defined as the time during which anode voltage falls from V_a to 0.9 V_a, where V_a is the initial value of anode voltage.
- ➢ The gate current has non-uniform distribution of current density over cathode surface due to p-layer.
- ➢ Its value is much higher near the gate but decreases rapidly as the distance from the gate increases.
- ➢ It shows that during t_d, anode current flows in a narrow region near the gate where gate current density is highest.



♣ **Rise Time (t_r): -**

- ➢ It is the time required for anode current to rise from 10 to 90%.
- ➢ It can also be defined as the time required for forward blocking off-state voltage to fall from 0.9 to 0.1 of its initial value-OP. This is inversely proportional to magnitude of gate current & its build up rate.
- ➢ Thus, t_r can be minimized if high and steep current pulses are applied to the gate.
- ➢ For series RL circuit, the rate of rise of anode current is slow, therefore, t_r is more and for the RC series circuit, di/dt is high thus t_r is less. During rise-time, turn-on losses are the highest due to high anode voltage V_a and large anode current I_T occurring together in the Thyristor.

♣ **Spread-Time (t_s)**: -

- The spread time is the time required for the forward blocking voltage to fall from 0.1 to its value to the on-state voltage drop (1 to 1.5 V). After the spread time, anode current attains steady-state values and the voltage drop across SCR is equal to the on-state voltage drop of the order of 1 to 1.5 V

♣ **Turn-on Time (t_{on})**: -

- This is the sum of the delay time, rise-time and spread time. This is typically of the order of 1 to 4 μs, depends upon the anode circuit parameters and the gate signal wave shapes.
- The width of the firing pulse should, be more than 10 μs, preferably in the range of 20 to 100 μs.
- The amplitude of the gate-pulse should be 3-5 times the minimum gate current required to trigger SCR.
- From fig, it is noted that during rise-time, the SCR carries a large forward current and supports an appreciable forward voltage. This may result in high instantaneous power dissipation creating local internal hot-spots which could destroy the device.
- It is, therefore, necessary to limit the rate of rise of current. Normally, a small inductor, called di/dt inductor is inserted in the anode circuit to limit the di/dt of the anode current.
- The shadow area under the power-curve in Fig. represents the switching loss of the device.
- This loss may be significant in high-frequency applications.

Ψ Dynamic TURN-OFF Switching Characteristics of SCR: -

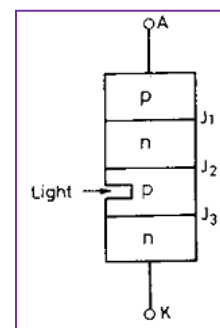
- Once the SCR starts conducting an appreciable forward current, the gate has no control on it and the device can be brought back to the blocking state only by reducing the forward current to a level below that of the holding current. Process of turn-off is also called as **Commutation**.
- There are various methods used for turning off Thyristor.
- However, if a forward voltage is applied immediately after reducing the anode current to zero, it will not block the forward voltage & will start conducting again, although it is not triggered by a gate pulse.
- Therefore, it is necessary to keep the device reverse biased for a finite period before a forward anode voltage can be reapplied.
- The turn-off time of the Thyristor is defined as the minimum time interval between the instant at which the anode current becomes zero, and the instant at which device is capable of blocking the forward voltage. The total turn-off is the sum of the reverse, recovery time (t_{rr}) & gate recovery time (t_{gr}).
- At the instant t_1, the anode forward current becomes zero.
- During the reverse recovery time t_1 to t_3, the anode current flows in the reverse direction.
- At the instant t_2, a reverse anode voltage is developed and the reverse recovery current continuous to decrease. At t_3, junction J_1 & J_3 are able to block a reverse voltage.
- However the Thyristor is not yet able to block a forward voltage because carriers, called *trapped charges,* are still present at junction J_2. During the interval t_3 to t_4, these carriers recombine.
- At t_4 recombination is complete and therefore, a forward voltage can be reapplied at this instant.
- The SCR turn-off time is the interval between t_4 to t_1. Thus, the **total turn-off time** (t_q) required for the device is the sum of the duration for which the reverse recovery current flows after the application of reverse voltage and the time required for the recombination of all excess carriers in the inner two layers of the device. For highly inductive load circuit, the current cannot change abruptly at t_1.
- Also, the fast change in current at t_2 may give rise to high voltage surges in the inductance, which will then appear across the terminals of the Thyristor.

❖ TURN-ON METHODS OF A THYRISTOR : -

- When anode is positive w.r.t. cathode, a Thyristor can be turned on. A Thyristor can be switched from a non-conducting state to a conducting state in several ways described as follows: -

Ψ Forward Voltage Triggering : -

- When anode-to-cathode forward voltage is increased with gate circuit open, the reverse biased junction J_2 will have an avalanche breakdown at a voltage called forward breakover voltage (V_{BO}).



- At this stage, a Thyristor changes from OFF state (High voltage with low leakage current) to ON-state (low voltage with large forward current).
- The forward voltage-drop across the SCR during the ON state is of the order of 1 to 1.5 V and increases slightly with load current.

Ψ Thermal Triggering (Temperature Triggering): -

- Like any other semiconductor, the width of the depletion layer of a Thyristor decreases on increasing the junction temperature. Thus, in a Thyristor when the voltage is applied between the anode & cathode is very near to its breakdown voltage, the device can be triggered by increasing junction temperature.
- By increasing the junction temperature to a certain value (within the specified-limit), a situation comes when the reverse biased junction collapses making the device conduct.
- This method of triggering the device by heating is known as the thermal triggering process.

Ψ Radiation Triggering (Light Triggering): -

- In this method, as the name suggests, the energy is imparted by radiation. Thyristor is bombarded by energy particles such as neutrons or photons. With the help of this external energy, electron-hole pairs are generated in the device, thus increasing the number of charge carriers.
- This leads to instantaneous flow of current within the device and the triggering of the device.
- For radiation triggering to occur, the device must have high value of rate of change of voltage (dv/dt).
- Light activated silicon controlled rectifier (LASCR) and light activated silicon controlled switch (LASCS) are the examples of this type of triggering.

Ψ dv/dt Triggering: -

- We know that with forward voltage across the anode and cathode of a device, the junctions J_1, and J_3 are forward biased, whereas the junction J_2 becomes reverse biased. This reverse biased junction J_2, has the characteristics of a capacitor due to charges existing across the junction.
- If a forward voltage is suddenly applied, a charging current will flow tending to turn the device ON.
- If the voltage impressed across the device is denoted by V, the charge by Q and the capacitance by C_j,

  then $i_C = \frac{dQ}{dt} = \frac{d}{dt}(C_j V) = C_j \frac{dV}{dt} + V \frac{dC_j}{dt}$ $\quad$ $i_C = C_j \frac{dV}{dt}$

- The rate of change of junction capacitance may be negligible as the junction capacitance is almost constant. The contribution to charging current by the later term is negligible. Hence, ⇧
- Therefore, if the rate of change of voltage across the device is large, the device may tum-on even though the voltage appearing across the device is small.

Ψ Gate Triggering

- This is the most commonly used method for triggering SCRs. In laboratories, almost all the SCR devices are triggered by this process. By applying a positive signal at the gate terminal of the device, it can be triggered much before the specified break over voltage.
- The conduction period of the SCR can be controlled by varying the gate signal within the specified values of the maximum and minimum gate currents.
- For gate triggering, a signal is applied between the gate and the cathode of the device.
- **Three** types of signals can be used for this. They are either d.c. signals, pulse signals or ac signals.

D.C. Gate Triggering: -

- In this type of triggering, a d.c. voltage of proper magnitude and polarity is applied between the gate and the cathode of the device in such a way that the gale becomes positive with respect to the cathode.
- When the applied voltage is sufficient to produce required gate current, the device starts conducting.
- One drawback of this scheme is that both the power and control circuits are d.c. and there is no isolation between the two. Another disadvantage of this process is that a continuous d.c. signal has to be applied, at the gate causing more gate power loss.

A.C. Gate Triggering: -

- A.C. source is most commonly used for the gate signal in all application of thyristor control adopted for a.c. applications. This scheme provides the proper isolation between the power and the control circuits.
- The firing angle control is obtained very conveniently by changing the phase angle of control signal.

- However, the gate drive is maintained for one half cycle after the device is turned ON, and a reverse voltage is applied between the gate and the cathode during the negative half cycle.
- The drawback of this is that a separate transformer is required to step down a.c. supply, which is costly.

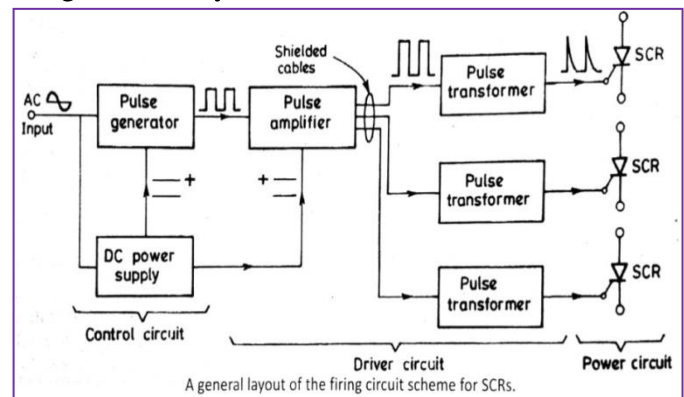
Pulse Gate Triggering : -

- This is the most popular method for triggering the device. In this method, the gate drive consists of a single pulse appearing periodically or a sequence of high frequency pulses.
- This is known as carrier frequency gating. A pulse transformer is used for isolation.
- The main advantage of this method is that there is no need of applying continuous signals and hence, the gate losses are very much reduced.
- Electrical isolation is also provided between the main device supply and its gating signals.

General functions to be fulfilled by Gate Control Circuits: -

- The gate control circuit is also called the firing circuit and it should fulfill the following two functions:-
- ♣ If power circuit has more than one SCR, the firing circuit should produce gating pulses for each SCR at the desired instant for proper operation of the power circuit. These pulses must be periodic in nature and the sequence of firing must correspond with the type of thyristorised power controller.
- ♣ Before giving the voltage pulses to the firing circuit, the voltage pulses should be fed to a driver circuit. The reason is that the control signal generated by a firing circuit may not be able to turn-on the SCR.

FIRING CIRCUITS: -



A general layout of the firing circuit scheme for SCRs.

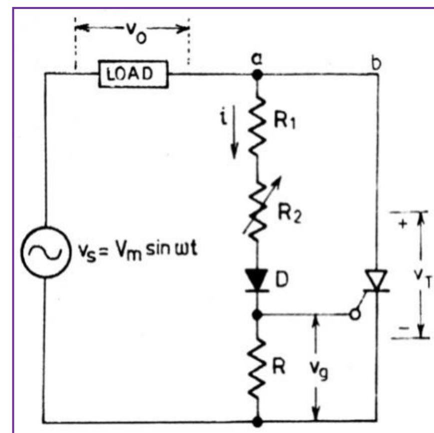
- An SCR can be switched from off-state to on-state in several ways; these are forward-voltage triggering, dv/dt triggering, temperature triggering, light triggering and gate triggering etc.
- The instant of turning on the SCR cannot be controlled by the first three methods listed above.
- Light triggering is used in some applications, particularly in a series connected string.
- Gate triggering is, however, the most common method of turning on the SCRs, because this method lends itself accurately for turning on the SCR at the desired instant of time. In addition, gate triggering is an efficient and reliable method. Here, the firing circuits for SCR are studied in detail.

Ψ Main Features of Firing Circuits: -

- As stated above, the most common method for controlling the onset of conduction in an SCR by means of gate voltage controls. The gate control circuit is also called **firing**, or triggering, circuit.
- These gating circuits are usually low-power electronic circuits.
- A firing circuit should fill following 2 functions : -
  (i) If power circuit has more than one SCR, the firing circuit should produce pulses for each SCR at the desired instant for proper operation of the power circuit. These pulses must be periodic in nature.
  (ii) The control signal generated by a firing circuit may not be able to turn-on an SCR. It is, therefore, common to feed the voltage pulses to a *driver circuit* and then to gate circuit. A driver circuit consists of a pulse amplifier and a pulse transformer.
- A firing circuit scheme, in general, consists of the components shown in Fig.
- A regulated dc power supply is obtained from an ac voltage source. Pulse gene supplied from both AC & DC sources, gives out voltage pulses which are then fed to amplifier for amplification.
- Shielded cables transmit the amplified pulses to transformers. The function of pulse transformer is to isolate the low-voltage gate-cathode circuit from the high-voltage anode-cathode circuit.
- Some firing circuit scheme described in this section as follows.
- The different FIRING Circuits used are: -
  - ♣ R-Firing Circuit
  - ♣ RC-Firing Circuit
  - ♣ Synchronous Triggering (Ramp Triggering) Circuit
  - ♣ UJT Pulse Trigger Circuit

Resistance (R) -Firing Circuit: -

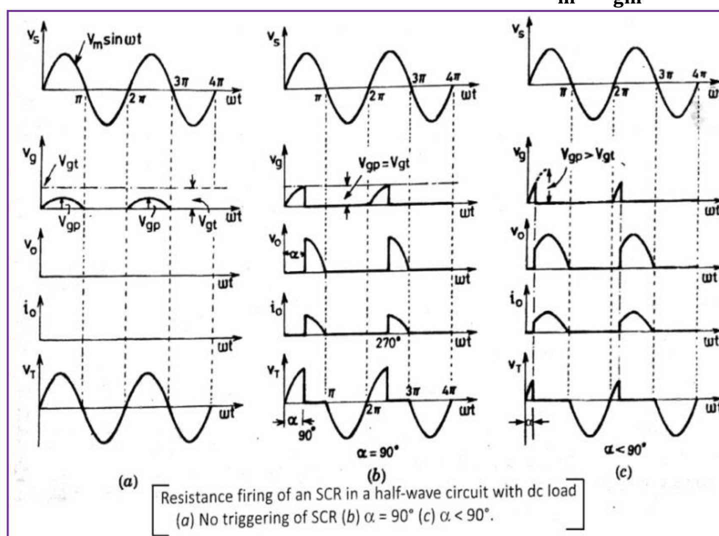
- R and RC firing circuits are not in commercial use these days.



- These are presented here for the sake of highlighting the basic principles of triggering the SCRs.
- They offer simple and economical firing circuits.
- **Resistance Trigger** circuits are the simplest & most economical.
- They however, suffer from a limited range of firing angle control (0^0 to 90°), great dependence on temperature and difference in performance between individual SCRs.
- Fig. shows the most basic resistance triggering circuit. R_2 is the variable resistance, R is the stabilizing resistance.
- When R_2 = zero, gate current may flow from source, through load, R_1, D & gate to cathode. This current should not exceed maximum permissible current I_{gm}. So R_1 can be found from the relation,

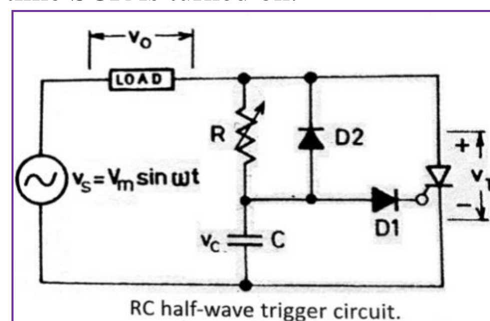
  $\frac{V_m}{R_1} \le I_{gm}$ or $R_1 \ge \frac{V_m}{I_{gm}}$ Where, V_m = maximum value of source voltage.
- It is thus seen that function of R_1 is to limit the gate current to a safe value as R_2 is varied.
- Resistance R should have such a value that maximum voltage drop across it does not exceed maximum possible gate voltage V_{gm}. This can happen only when R_2 is zero. Under this condition,

  $\frac{V_m}{R_1 + R}.R \le V_{gm}$ ➔ $V_m.R \le V_{gm}(R_1 + R)$ ➔ $V_m.R - V_{gm}R \le V_{gm} R_1$ ➔ $\mathbf{R \le \frac{V_{gm}.R_1}{V_m - V_{gm}}}$



Resistance firing of an SCR in a half-wave circuit with dc load (a) No triggering of SCR (b) α = 90° (c) α < 90°.

- As resistance R_l, R_2 are large, gate trigger circuit draws a small current.
- Diode D allows the flow of current during positive half cycle only, i.e. gate voltage v_g is half-wave dc pulse.
- The amplitude of this de pulse can be controlled by varying R_2.
- The potentiometer setting R_2 determines the gate voltage amplitude.
- When R_2 is large, current $\boldsymbol{i}$ is small & voltage across R, i.e. $v_g = i$. R is also small as shown in Fig. (a).
- As V_{gp} (peak gate voltage v_g) is less than V_{gt} (gate trigger voltage), SCR will not Turn ON.
- Therefore, load voltage v_o = 0, i_o = 0 and supply voltage v_s appears as v_t across SCR shown in Fig. (a).
- Note that trigger circuit consists of resistances only, v_g is therefore in-phase with source voltage v_s.
- In Fig. (b), R_2 is adjusted such that $V_{gp} = V_{gt}$. This gives the value of firing angle as 90°.
- Various current & voltage waveforms are shown in fig.
- In Fig. (c), $V_{gp} > V_{gt}$. As soon as v_g becomes equal to V_{gt} for first time SCR is turned on.
- The resistance triggering cannot give firing angle beyond 90°.
- Increasing v_g above V_{gt} turns ON the SCR at firing angles < 90°
- When v_g reaches V_{gt} for first time, SCR fires, gate loses control & v_g is reduced to almost zero (about 1V) value as shown.



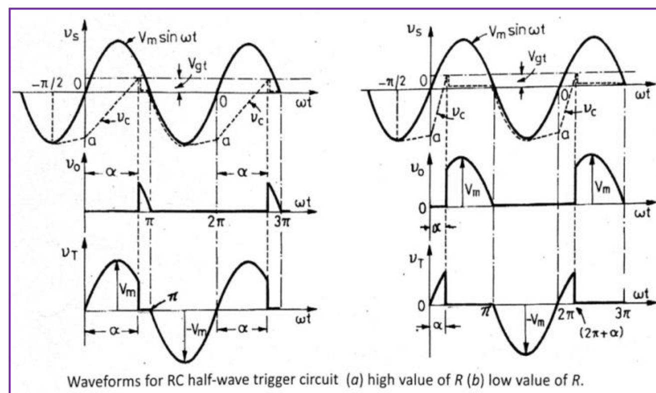
RC half-wave trigger circuit.

Resistance – Capacitance Firing Circuit: -

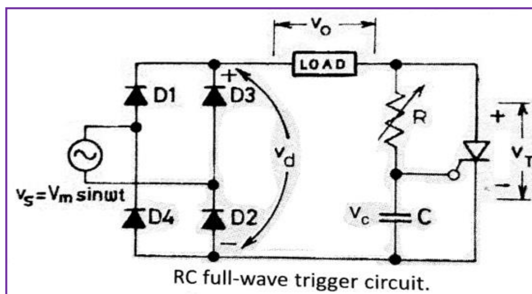
- The limited range of firing angle control by R-Firing circuit can overcome by RC-Firing circuit. There are several types of RC trigger circuit. Here only two of them are presented.

♣ RC Half-Wave Trigger Circuit: -

- Fig. shows RC half-wave trigger circuit. By varying **R**, firing angle can be controlled from 0° to 180°.
- In the negative half cycle, capacitor C charges through D_2 with lower plate positive to the peak supply voltage V_m at ωt = - 90°.
- After ωt = 90°, source voltage v_S decreases from – V_m at ωt = - 90° to zero at ωt = 0°. During this period, capacitor voltage v_c may fall from -V_m at ωt = - 90° to some lower value **-oa** at ωt=0° as Fig.


Waveforms for RC half-wave trigger circuit (a) high value of R (b) low value of R.

- Now As **SCR** anode voltage passes through zero and becomes positive, C begins to charge through variable resistance R from initial voltage oa.
- When capacitor charges to +ve voltage equal to gate trigger voltage V_{gt}, SCR is fired.
- After this, capacitor holds to a small +ve voltage.
- Diode D1 is used to prevent breakdown of cathode to gate junction through D_2 during -ve half cycle.
- An examination reveals that firing angle can never be zero and 180^0.
- The SCR will trigger when $\mathbf{v_c = V_{gt} + v_d}$,
- Where $\mathbf{v_c}$ = Capacitor Voltage, $\mathbf{V_{gt}}$ = Gate trigger Voltage and $\mathbf{v_d}$ = Voltage Drop across diode D_1.

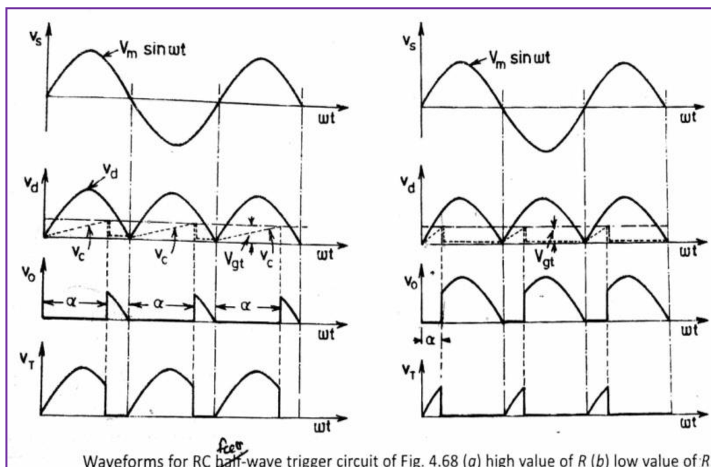


RC full-wave trigger circuit.

- At the instant of triggering, if v_c is assumed constant, the current I_{gt} must be supplied by voltage source through R, D_1 and gate to cathode circuit. Hence maximum value of R is obtained by

  ➔ $v_s \geq RI_{gt} + v_c$ ➔ $v_s \geq RI_{gt} + V_{gt} + v_d$

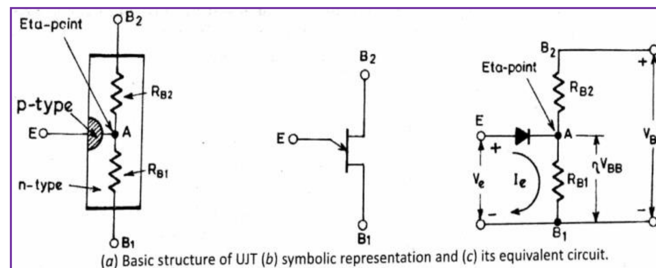
  ➔ $\mathbf{R \leq \frac{v_s - V_{gt} - v_d}{I_{gt}}}$
- v_s is source voltage at which Thyristor can be ON.
- In Fig (a), R is more, the time taken for C to charge from - oa to $(V_{gt} + v_d) \equiv V_{gt}$ is more, firing angle is more and thus average output voltage is low.
- In Fig (b), R is less, firing angle is low and therefore average output voltage is more.


Waveforms for RC ~~half~~ full-wave trigger circuit of Fig. 4.68 (a) high value of R (b) low value of R.

♣ RC Full - Wave Trigger Circuit: -

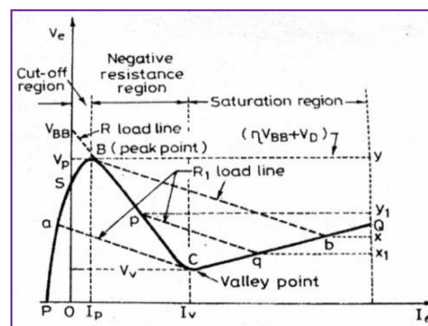
- A simple RC trigger circuit giving full-wave output voltage is shown in Fig.
- Diodes D_1-D_4 forms a full-wave diode bridge.
- In this circuit, the initial voltage from which the capacitor C charges is almost zero.
- The capacitor C is set to this low +ve voltage (upper plate +ve) by clamping action of SCR gate.
- When capacitor charges to a voltage equal to V_{gt}, SCR triggers & rectified voltage v_d appears across load as v_o. The value of RC is calculated by the empirical relation. $\mathbf{R \leq \frac{v_s - V_{gt}}{I_{gt}}}$ **.** In fig (a), firing angle (**α**) more than 90° and in Fig. (b), α < 90°.

UJT < Uni-Junction Transistor >: -

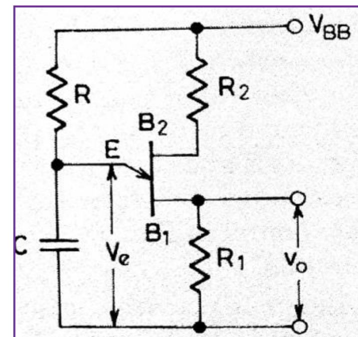


(a) Basic structure of UJT (b) symbolic representation and (c) its equivalent circuit.

- R & RC triggering circuits give prolonged pulses.
- Hence, power dissipation in gate circuit is large.
- At the same time, R & RC triggering ckt cannot be used for automatic or feedback control systems.
- These difficulties can be overcome by use of UJT triggering circuits. Pulse triggering is preferred as it offers several merits over R & RC.
- Pulses can be adjusted easily to suit such a wide spectrum of gate characteristics.
- The power level in pulse triggering is low as the gate drive is discontinuous; pulse triggering is therefore more efficient.
- As pulses with higher gate current are permissible, pulse firing is more reliable and faster. First we will study UJT then we will use as relaxation Oscillator for triggering SCRs. **[V-I of UJT→]**

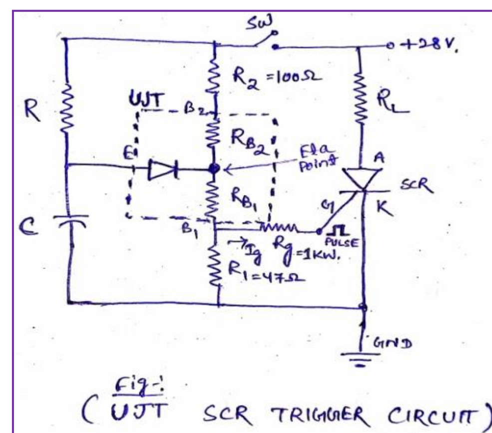


- An UJT is made up of an n-type silicon base to which p-type emitter is embedded Fig. (a).
- The n-type base is lightly doped whereas p-type is heavily doped.
- The two ohmic contacts provided at each end are called base-one B_1 and base-two B_2.
- So, an UJT has three terminals, namely the emitter E, base-one B_1 and base-two B_2.
- Between bases B_1 and B_2, the uni-junction behaves like an ordinary resistance.
- R_{B1} and R_{B2} are the internal resistance respectively from bases B_1 and B_2 to **eta-point** A as in fig. (a).
- It's symbolic representation given in Fig. (b) and its equivalent circuit in Fig. (c).
- When a voltage V_{BB} is applied across the two base terminals B_1 and B_2,
- The potential of point A w. r. t B_1 is given by $V_{AB1} = \frac{R_{B1} \cdot V_{BB}}{R_{B1}+R_{B2}} = \eta\, V_{BB}$
- Where $\eta = \frac{R_{B1}}{R_{B1}+R_{B2}}$ = **Intrinsic Standoff Ratio.**
- $R_{BB} = R_{B1} + R_{B2}$ = Interbase resistance (5-10kΩ)



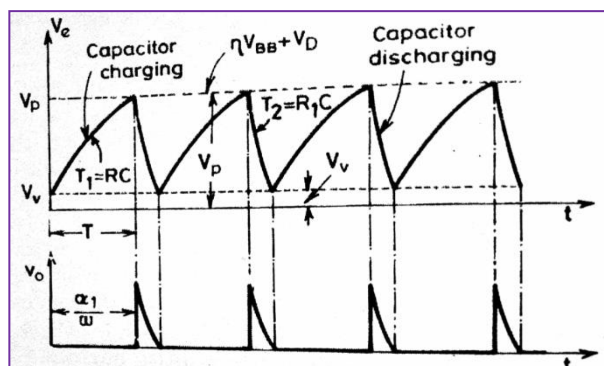
UJT Oscillator Triggering Circuits: -

- The UJT is often used as a trigger device for SCRs and TRIACs.
- Other applications include non-sinusoidal oscillators, sawtooth generators, phase-control, and timing circuits etc.
- The most common UJT circuit in use today is relaxation oscillator shown in Fig.
- Since UJT exhibits –ve resistance characteristics. Also, this type of circuit is basic to other timing and trigger circuit.
- As its switching time is in the range of nanoseceonds.
- The external resistances R_1, R_2 are small in comparison with internal resistances R_{B1}, R_{B2} of UJT bases.
- Charging resistance R should be such that its load line intersects thr device characteristics only in -ve resistance region.
- In above Fig., when source voltage V_{BB} is applied, capacitor C begins to charge through R exponentially towards V_{BB}.
- During this charging, emitter circuit of UJT is an open circuit.



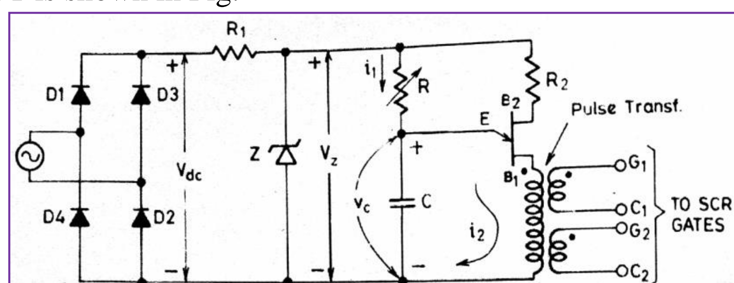
- The capacitor voltage v_c equal to emitter voltage v_e, is given by, $\boldsymbol{v_c = v_e = V_{BB}\,(1 - e^{-t/RC})}$
- The time constant of the charge circuit is τ_1 = RC. When emitter voltage v_e (or v_c) reaches the peak-point voltage V_p (= $\eta V_{BB} + V_D$), the junction between E - B_1 breaks down.
- As a result, UJT turns on and capacitor C rapidly discharges through low resistance R_1 with a time constant $\tau_2 = R_1C$. Here τ_2 is much smaller than τ_1.
- The voltage drop across R_1, equal to v_0, is applied to gate-cathode circuit of an SCR to turn it on.
- When the emitter voltage decays to the valley-point voltage V_V, emitter current [$V_V/(R_{B1} + R_1)$] falls below I_V and UJT turns off.
- The time T required for capacitor C to charge from initial voltage V_V to peak-point voltage V_P, through large resistance R, can be $\mathbf{V_P = \eta\, V_{BB} + V_D}$.
- The Value of firing angle is given by

$$\alpha_1 = \omega T = \omega RC \ln [1/(1-\eta)]$$

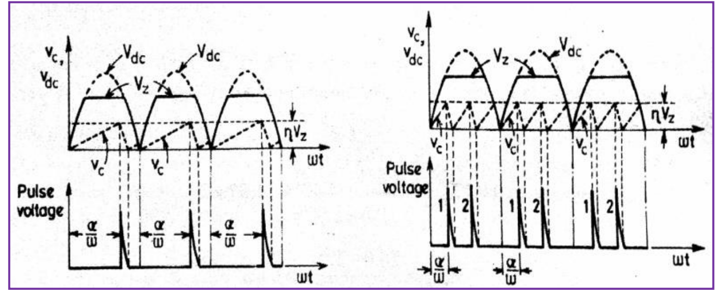


Synchronized UJT Triggering Circuits <or RAMP Triggering> : -

- A synchronized UJT trigger circuit using an UJT is shown in Fig.
- Diodes D_1 - D_4 rectify ac to dc.
- Resistor R_1 lowers V_{dc} to a suitable value for the zener diode and UJT.
- Zener diode Z functions to clip the rectified voltage to a standard level V_z, which remains constant except near the V_{dc} zero as in Fig.



- This voltage V_z is applied to the charging circuit RC. Current i_1 charges capacitor C at a rate determined by R. Voltage across capacitor is marked by v_c in Fig.
- When voltage v_c reaches the unijunction threshold voltage ηV_z, the E - B_1 junction of UJT breaks down and the capacitor C discharges through primary of pulse transformer sending current i_2 as shown in Fig.



- As the current i_2 is in the form of pulse, windings of pulse transformer have pulse voltages at their secondary terminals.
- Pulses at the two secondary windings feed the same in-phase pulse to two SCRs of a full-wave circuit.
- SCR with positive anode voltage would turn on.
- As soon as the capacitor discharges, it starts to recharge as shown. Rate of rise capacitor voltage can be controlled by varying R. The firing angle can be controlled up to about 150^0.
- This method of controlling the output power by varying charging resistor R called **ramp control**, open-loop control or manual control.
- As the zener diode voltage V_z goes to zero at the end of each half cycle, the synchronization of the trigger circuit with the supply voltage across SCRs is achieved.
- Thus the time t, equal to **α/ω**, when the pulse is applied to SCR for the first time, will remain constant for the same value of R.
- Small variations in the supply voltage and frequency are not going to effect the circuit operation.
- In case R is reduced so that v_c reaches UJT threshold voltage twice in each half cycle, then there will be two pulses in each half cycle as shown in fig.
- As the first pulse will be able to turn-on the SCR, second pulse in each cycle is redundant.

❖ TURN-OFF METHODS (Communication Schemes)

- A Thyristor is Turned-ON by applying a signal to its gate-cathode circuit. For the purpose of power control or power conditioning, a conducting thyristor must be Turned-OFF as desired.
- As the Turn-OFF of a Thyristor means bringing the device from forward conduction state to forward blocking state. Thyristor Turn-Off requires that : - **(a)** Its anode current falls below the holding current & **(b)**A reverse voltage is applied to thyristor for sufficient time to enable it to recover to blocking state.
- **Commutation** is defined as the process of **Turning-OFF** a Thyristor.
- Once thyristor starts conducting, gate loses control over the device, therefore, external means may have to be adopted to commutate the thyristor. Several commutation techiques are adopted for this purpose.
- The two methods by which a Thyristor can be commutated are as follows: -

Ψ Natural Commutation: -

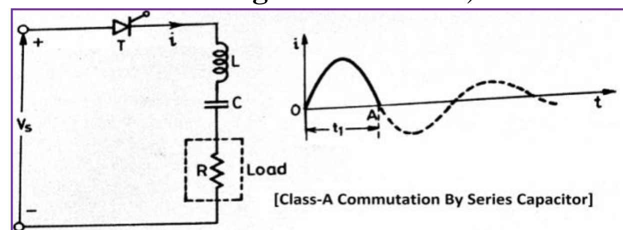
- The simplest and most widely used method of commutation makes use of the alternating, reversing nature of a.c. voltages to effect the current transfer.
- We know that in a.c. circuits, the current always passes through zero every half cycle.
- As current passes through natural zero, a reverse voltage will mulluncously appear across the device.
- This immediately turns-off the device. This process is called as **Natural Commutation** since no external circuit is required for this purpose.
- This method may use a.c. mains supply voltages or the a.c. voltages generated by local rotating machines or resonant circuits. The line comutated converters and inverters come under this category.

Ψ Forced Commutation: -

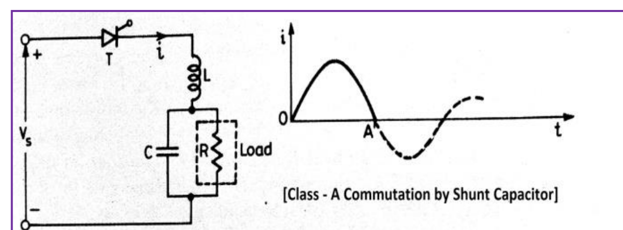
- Once Thyristors are operating in the ON state, carrying forward current, it can turned OFF by reducing current flowing through them to zero for sufficient time to allow the removal of charged carriers.
- In case of d.c. circuits, for switching off the thyristors, the forward current should be forced to be zero by means of some external circuits. The process is called **Forced Commutation** and external circuits required for it are known as **commutation circuits**. The components (inductance, and capacitance) which constitute the commutating circuits are called as **Commutating Components**.
- A reverse voltage is developed across the device by means of a commutating circuit that immediately brings the forward current in the device to zero, thus Turning-OFF the device.

- Producing reliable commutation is a difficult problem to be tackled while designing chopper and inverter circuits. The most important stage in the designing process is choosing a forced Turn-OFF methode and deciding its components.
- The classification of the methods of forced commutation is based on the arrangement of commutating components and the manner in which zero current is obtained in the SCR.
- There are six basic methods of commutation by which thyristors may be turned OFF.
  - **CLASS - A** (**Load** Commutation or **Resonant** Commutation or **Self** Commutation)
  - **CLASS - B** (**Resonant-Pulse** Commutation)
  - Class - C (**Complementary** Commutation)
  - Class - D (**Impulse** Commutation or **Auxilary** Commutation or **Voltage** Commutation)
  - Class - E (**External Pulse** Commutation)
  - Class - F (**Line** Commutation)

Load < Class - A> Commutation:-

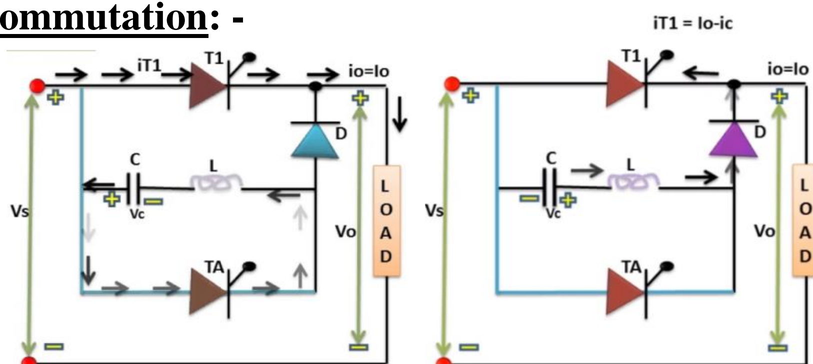


- For achieving **Load** commutation of a Thyristor, the commutating components L & C are connected as shown in Fig. Here R is the Load resistance.
- For low value of R, L and C are connected in series with R, Fig. (a). For high value of R, load R is connected across Fig. (b).

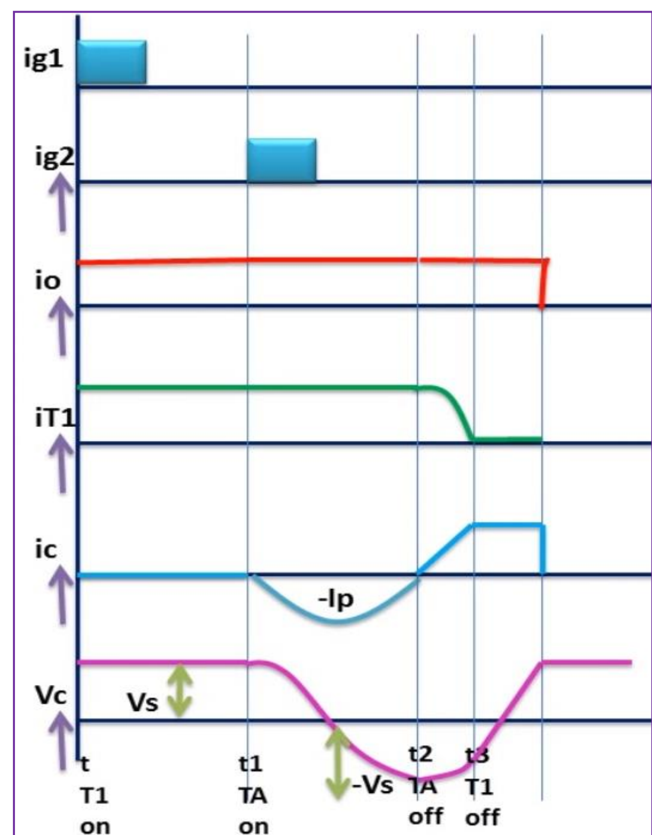


- The essential requirement for both the circuits of Fig. is that the over circuit must be under damped.
- When these circuits are energized from dc, current waveform, as shown on the right hand side of Fig. are obtained. It is seen that current is first arises maximum value and then begins to fall.
- When current decays to zero and tends to reveres Thyristor in fig. is turned-off on its own at instant A.
- **Load** or Class - A commutation is prevalent in Thyristor circuits supplied from a source.
- The nature of the circuit should be such that when energized from a dc source current must have a natural tendency to decay to zero for the load commutation to occur Thyristor circuit.
- Load commutation is possible in de circuits and not in ac circuits.
- Class - A or Load Commutation is also called **Resonant Commutation** or **Self-Commutation**.

Resonant-Pulse <Class - B> Commutation: -



- For explaining class-B, or resonant-pulse communication, refer to Fig.
- In this figure, source voltage V_S charges capacitor C to voltage V_S with left hand plate positive.
- Main thyristor Tl as well as auxiliary thyristor TA are off.
- Positive direction of capacitor voltage v_c and capacitor current i_c are marked.
- When Tl is turned on at t = 0, a constant current I_0 is established in the load circuit.
- Here, for simplicity, load current is assumed constant.
- Upto time t_1, $v_c = V_S$, $i_c = 0$, $i_0 = i_{T1}$ and $i_{T1} = I_0$.
- For initiating the commutation of main thyristor Tl, auxiliary thyristor TA is gated at $t = t_1$ With TA on, a resonant current i_c begins to flow from C through TA, L and back to C.
- This resonant current, with time measured from instant t_l is given by $i_c = -V_S\sqrt{\frac{C}{L}}\sin\omega_0 t = -I_P \sin\omega_0 t$
- Minus sign before $I_P \sin\omega_0 t$ is due to the fact that this current flows opposite to the reference positive direction chosen for i_c in Fig. (a). Capacitor voltage, $v_c = \frac{1}{C}\int i_c dt = V_S \cos\omega_0 t$
- After half a cycle of i_c, from instant t_1 ; $i_c = 0$, $v_c = -V_S$ and $i_{T1} = I_0$, After π radians from instant t_1, i.e. just after instant t_2, as i_c tends to reverse, TA is turned off at t_2.



- With v_c = - V_S, right-hand plate has positive polarity. Resonant current i_c now builds up through C, L, D and T1. As this current i_c grows opposite to forward thyristor current of Tl, net forward current $\boldsymbol{i_{T1} = I_0 - i_c}$ begins to decrease.
- Finally, when i_c in the reversed direction attains the value I_0, forward current in Tl ($i_{T1} = I_0 - I_0 = 0$) is reduced to zero and the device Tl is turned off at t_3.
- For reliable commutation, peak resonant current I_P must be greater than load current I_0.
- As thyristor is commutated by the gradual build up of resonant current in the reversed direction, this method is also called **current commutation**, **class B commutation** or **resonant-pulse commutation**.
- After Tl is turned off at t_3, constant current I_0 flows from V_S to load through C, L and D.
- Capacitor begins charging linearly from $-V_{ab}$ to zero at t_4 and then to V_S at t_5.
- As a result, instant t_5, when $v_c = V_S$, load current $i_0 = i_c = I_0$ reduces to zero as shown.
- It is seen from the waveform of i_c that main thyristor Tl is turned off when

  $V_S\sqrt{\frac{C}{L}}\sin\omega_0 t(t_3 - t_2)$ or $\omega_0(t_3 - t_2) = \sin^{-1}\frac{I_P}{I_0}$ where

  $I_P = V_S\sqrt{\frac{C}{L}}$ = peak resonant current.
- Main thyristor TI is commutated at t_3. As constant load current I_0 charges C linearly from - V_{ab} at t_3 to zero at t_4, SCR TI is reverse biased by voltage v_c for a period $(t_4 - t_3) = t_c$. ➔ $t_c = t_4 - t_3 = C\frac{V_{ab}}{I_0}$
- Eq. shows that t_c is dependent on the load current.
- Waveform of capacitor voltage v_c reveals that the magnitude of reverse voltage V_{ab} across main thyristor TI, when it gets commutated, is given by $\mathbf{V_{ab} = V_S \cos\omega_0(t_3 - t_2)}$.

♣ Another method of classification of Thyristor commutation techniques are:-

- ✓ Line commutation: Class F
- ✓ Load commutation: Class A
- ✓ Forced commutation: Class B, C & D
- ✓ External-pulse commutation: Class E
- In **Line** or Natural, commutation, natural reversal of ac supply voltage commutates the conducting Thyristor.
- As stated before, line commutation is widely used in ac voltage controllers, phase-controlled rectifiers and step-down Cycloconverter.
- In **Load** Commutation, L and C are connected in series with the load or C in parallel with the load such that overall load circuit is under damped.

SN	TRANSISTOR	THYRISTOR
1.	Transistor is Three layer, Two junction device.	Thyristor is a Four layer, Three junction device.
2.	To keep a Transistor in the conducting state, a continuous, base current is required.	Thyristors require a pulse to make it conducting and thereafter it remain conducting.
3.	When it conduct appreciable current, the forward voltage drop is of the order of 0.3 to 0.8 V.	The forward voltage drop across the device is of the order of 1.2 to 2V.
4.	The voltage and current ratings of Transistors available at present are not high.	Thyristors with very high voltage and current ratings are available
5.	Transistors have no surge current capacity & can withstand only a low rate of change of current.	Thyristors have surge-current rating, thus it can withstand high rate of change of current.
6.	Commutation circuitry, which is costly and bulky, is not required.	Commutation circuit is required.
7.	Power-transistors can be used in very high-frequency applications.	Thyristors are used in comparatively low frequency applications
8.	Circuits using power transistors will be smaller in size and less costly compared to thyristors.	Comparatively larger in size and is costlier.
9.	There has been little operating experience in high power applications. Power transistors or Darlington pairs are more susceptible to failure.	Thyristor circuits, on the other hand, have a proven record of many years of reliable operation

- **Load** commutation is commonly employed in series inverters.
- In **Forced** commutation, commutating components L and C do not carry current continuously.
- So class B, C and D commutation constitute forced commutation techniques.
- As in forced commutation, forward current of the Thyristor forced to zero by external circuitry called commutation circuit. Forced commutation usually employed in dc choppers and inverters.

❖ RATINGS OF THYRISTORS

- All semiconductor devices have definite limits to their capability and exceeding these even for short times will result in failure, loss of control, or irreversible deterioration.
- All thyristors, therefore, have to be used within their limits and this must include extreme conditions as may exist during circuit faults and it must take into account load, supply system, temperature and environmental variations.
- If extreme condition are not precisely known and cannot be calculated, then appropriate safety margins have to be chosen to allow for the unknown factors.
- Correct safety margins can only be decided from practical operating experience.
- Therefore, the reliable operation of the device can be ensured only if its ratings are not exceeded under all operating conditions. The objective of this section is to discuss the various SCR ratings.

VOLTAGE RATING:-

- It is essential that the voltage capability of a thyristor is not exceeded during operation even for a very short period of time. Therefore, the voltage rating of the device should be high enough to withstand anticipated voltage transients as well as the repetitive OFF state and reverse-blocking voltages.
- The various ratings related to the voltage are discussed in this section.

1. Working peak-off state forward voltage (V_{DWM})
2. Repetitive peak-off state forward voltage (V_{DRM})
3. Non-repetitive peak-off-state forward voltage (V_{DSM})
4. Working Peak Reverse Voltage (V_{RWM})
5. Repetitive Peak Reverse Voltage (V_{RRM})
6. Non-repetitive Peak Reverse Voltage (V_{RSM})
7. On State Voltage (V_T)
8. Gate Trigger Voltage (V_{GT})
9. Voltage Safety Factor (V_f)
10. Forward dv/dt rating [Rate of rise of off state voltage]

CURRENT RATING:-

- The current carrying ability of the thyristor is determined by the temperature at its junction. Since the thyristor is made up of a semiconductor material, it's thermal capacity is, therefore, quite small.
- Hence, even for short over currents, the junction temperature may exceed the rated value and the device may be damaged. In this section, current ratings of SCR are discussed for both repetitive and non-repetitive type of current waveforms.

1. Average On-state Current (I_{TAV})
2. RMS On-state Current (I_{RMS})
3. I^2t Rating
4. *di/dt* Rating
5. Holding Current (I_H)
6. Latching Current (I_L)
7. Gate Current [Ig_{min} and Ig_{max}]
8. Surge Current Rating (I_{TSM}) (Non-repetitive, Peak-on State Current)

POWER RATING (Losses):-

- The power-generated in the junction region of a thyristor in a normal operation consists of the following components of dissipation.
  1) Forward-conduction **or** Forward Conduction Loss
  2) Turn-on switching **or** Turn-on Losses
  3) Turn-off or commutation **or** Turn-off Losses
  4) Forward and Reverse blocking **or** Forward and Reverse Blocking Losses
  5) Gate pulse triggering **or** Gate Power Loss (Pg_{av})

THERMAL RATING:-

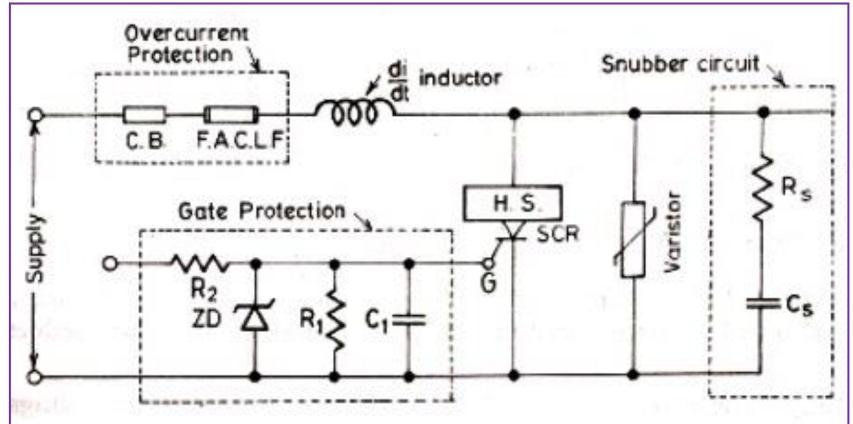
- The following are the main thermal ratings of the device.
  1. Junction Temperature (T_j)
  2. Transient Thermal Impedance (Z_{TH})

TURN-ON AND TURN-OFF TIME RATING: - Selecting a thyristor for a particular application is very much dependent on the turn-on and turn-off time. Fast switching thyristors have very low values of turn-on and turn-off time. This is achieved by gold doping in silicon.

❖ THYRISTOR PROTECTION: -

- Reliable operation of a thyristor demands that its specified ratings are not exceeded.
- In practice, SCR may be subjected to over voltage or over currents.
- During SCR Turn-on, di/dt may be prohibitively large.

- There may be false triggering of SCR by high value of dv/dt.
- A spurious signal across gate-cathode terminals may lead to unwanted turn-on.
- A SCR must be protected against all such abnormal conditions for satisfactory & reliable operation.
- SCRs are very delicate devices; therefore their protection against abnormal conditions is essential.
- The object of this section is to discuss various techniques adopted for the protection of SCR. **[C.B – Circuit Breaker, FACLF – Fast Acting Current Limiting Switch, H.S – Heat Sink, ZD – Zener Diode]**



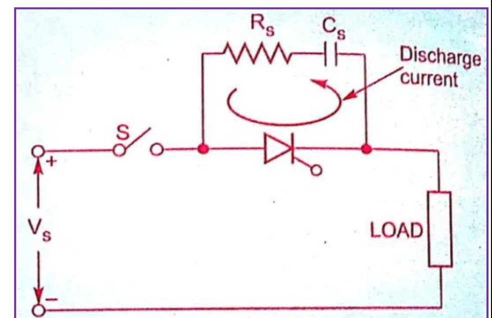
di/ dt Protection: -

- When a thyristor is forward biased and is turned on by a gate pulse, conduction of anode current begins in the immediate neighborhood of the gate-cathode junction.
- Thereafter, the current spreads across the whole area of junction.
- The thyristor design permits the spread of conduction to the whole junction area as rapidly as possible.
- However, if the rate of rise of anode current, i.e. di/dt, is large as compared to the spread velocity of carriers, local hot spots will be formed near the gate connection on account of high current density.
- This localized heating may destroy the thyristor. Therefore, the rate of rise of anode current at the time of turn-on must be kept below the specified limiting value.
- The value of di/dt can be maintained below acceptable limit by using a small inductor, called di/dt inductor, in series with the anode circuit. Typical di/dt limit values of SCRs are 20-500 A/μsec.
- Local spot heating can also be avoided by ensuring that the conduction spreads to the whole area as rapidly as possible. This can be achieved by applying a gate current nearer to (but never greater than) the maximum specified gate current.

(b) dv / dt Protection.

- It has already been discussed that if rate of rise of suddenly applied voltage across thyristor is high, the device may get turned on. Such phenomena of turning-on a thyristor, called dv/dt turn-on must be avoided as it leads to false operation of the thyristor circuit.
- For controllable operation of the thyristor, the rate of rise of forward anode to cathode voltage dv/dt must be kept below the specified rated limit. Typical values of dv/dt are 20-500 V/μsec.
- False Turn-on of SCR by large dv/dt can be prevented by using snubber circuit in parallel with device.

♣ DESIGN OF SNUBBER CIRCUITS: -



- A Snubber circuit consists of a series combination of resistance R_S and capacitance C_S in parallel with the thyristor as in Fig.
- Strictly speaking, a capacitor C_S in parallel with the device is sufficient to prevent unwanted **dv / dt** triggering of the SCR.
- When switch S is closed, a sudden voltage appears across the circuit. Capacitor C_S behaves like a short circuit, therefore voltage across SCR is zero.
- With the passage of time, voltage across C builds up at a slow rate such that dv/dt across C_S and thus across SCR is less than the specified maximum dv/dt rating of the device. Here the question arises that if C_S is enough to prevent accidental turn-on of the device by dv/dt, what is the need of putting R_S in series with C_S.
- Before SCR is fired by gate pulse, C, charges to full voltage V_S. When the SCR is turned on, capacitor discharges through SCR, & sends a current equal to V/ (Resistance of local path formed by C & SCR).
- As resistance is quite low, the turn-on di/dt will tend to be excessive & hence, SCR may be destroyed.
- In order to limit the magnitude of discharge current, a resistance R_S is inserted in series with C_S as Fig.

- When SCR is turned on initial discharge current V/R is relatively small and turn-on di/dt is reduced.
- In actual practice; R_S, C_S and the load circuit parameters should be such that dv/dt , across C, during its charging is less than the specified dv/dt rating of the SCR and discharge current at the turn-on of SCR is within reasonable limits.
- Normally, R_S, C_S and load circuit parameters form an under damped circuit so that dv/dt is limited to acceptable values. The design of Snubber circuit parameters is quite complex.
- In practice, designed Snubber parameters are adjusted up or down in the final assembled power circuit so as to obtain a satisfactory performance of the power electronics system.

Overvoltage Protection

- The thyristors are very sensitive to over voltage like other semiconductor devices.
- Over voltage transients are perhaps the main cause of thyristor failure.
- Transient over voltage cause either mal-operation of circuit by unwanted turn on of thyristor or permanent damage to the device due to reverse breakdown.
- A thyristor may be subjected to **Internal** or **External** over voltage.
- **Internal Over Voltages.** Large voltages may be generated internally during commutation of a SCR.
- After thyristor anode current reduces to zero, anode current reverses due to stored charges.
- This reverse recovery current rises to a peak value at which time the SCR begins to block.
- After this peak, reverse recovery current decays abruptly with large di/dt.
- Because of the series inductance L of the SCR circuit, large transient voltage Ldi/dt is produced.
- As this internal overvoltage may be several times the break over voltage of the device, the thyristor may be destroyed permanently.
- **External Over Voltages.** External over voltages are caused due to the interruption of current flow in an inductive circuit and also due to lightning strokes on the lines feeding the thyristor systems.
- When a thyristor converter is fed through a transformer, voltage transients are likely to occur when the transformer primary is energized or de-energized.
- Such over voltages may cause random turn on of a thyristor.
- As a result; the over voltages may appear across the load causing the flow of large fault currents.
- Over voltages may also damage the thyristor by an inverse breakdown.
- For reliable operation, the over voltages must be suppressed by adopting suitable techniques.

Over Current Protection

- Thyristors have small thermal time constants. Therefore, if a thyristor is subjected to over current due to faults, short circuits or surge currents; its junction temperature may exceed the rated value and the device may be damaged. There is thus a need for the over current protection of SCRs.
- As in other electrical systems, over current protection in thyristor circuits is achieved through the use of circuit breakers and fast-acting fuses as shown in fig.
- The type of protection used against over current depends upon whether supply system is weak or stiff.
- In a weak supply network, fault current is limited by the Source impedance below the multi-cycle surge current rating of the thyristor. In machine tool and excavator drives, if the motor stalls due to overloads, the current is limited by the source and motor impedances.
- The filter inductance commonly employed in de and ac drives may limit the rate of rise of fault current below the multi cycle surge current rating of the thyristor.
- For all such systems, over current can be interrupted by conventional fuses and circuit breakers.
- However, proper co-ordination is essential to guarantee that (i) fault current is interrupted before the thyristor is damaged and (ii) only faulty branches of the network are isolated.
- Conventional protective methods are, however, inadequate in electrical stiff supply networks.
- In such systems, magnitude and rate of rise of current is not limited because source has negligible impedance. As such, fault current and therefore junction temperature rise within a few milliseconds.
- Special fast-acting current-limiting fuses are, therefore, required for the protection of thyristors in these stiff supply networks.
- When both circuit breaker and fast-acting current-limiting fuse are used for over current protection of SCR, the faulty circuit must be cleared before any damage is done to the device.
- A circuit breaker has long tripping time, it is therefore generally used for protecting the semiconductor

device against the continuous overloads or against surge currents of long duration.

- An **F.A.C.L. fuse** is used for protecting thyristors against large surge currents of very short duration.
- The tripping time of the circuit breaker, the fusing-time of the fast-acting fuse must be properly co-ordinate with the rating of a thyristor. In order that fuse protects the thyristor reliably, the I^2t rating of the fuse must be less than that of the SCR.

Gate Protection

- Gate circuit should also be protected against over voltages and over currents.
- Over voltages across the gate circuit can cause false triggering of the SCR.
- Over current may raise junction temperature beyond specified limit leading to its damage.
- Protection against over-voltages is achieved by connecting a Zener diode ZD across the gate circuit.
- A resistor R2 connected in series with the gate circuit provides protection against over currents.
- A common problem in thyristor circuits is that they suffer from spurious, or noise, firing.
- Turning-on or turning-off of an SCR may induce trigger pulses in a nearby SCR. Sometimes transients in a power circuit may also cause unwanted signal to appear across the gate of a neighboring SCR.
- These undesirable trigger pulses may turn on the SCR leading to false operation of the main SCR.
- Gate protection against such spurious firing is obtained by using shielded cables or twisted gate leads.
- A varying flux caused by nearby transients cannot pass through twisted gate leads or shielded cables.
- As such no e.m.f. is induced in these cables and spurious firing of thyristors is thus minimized.
- A capacitor and a resistor are also connected across gate to cathode to bypass the noise signals.
- The capacitor should be less than 0.1 μF and must not deteriorate the wave shape of the gate pulse.

---- ALL THE BEST ---- ALL THE BEST ----

VERY SHORT TYPE QUESTIONS

1) Define Latching current and Holding current of SCR.
2) Write the full forms of IGBT, SMPS, TRC and BTBF.
3) Write down the applications of power diode.
4) What are the different types of Power Transistor?
5) Write any two application of TRIAC.
6) Draw the symbols of SCR, GTO and Power MOSFET.
7) Define turn-on time of SCR.
8) Write down the application of IGBT.
9) Draw the circuit symbol of power MOSFET and IGBT.
10) List applications of TRIAC.
11) Draw V-I Characteristics of Power, Signal and Ideal Diode.
12) Define Holding Current and Latching Current.
13) Differentiate between DIAC and TRIAC.
14) Define Holding current and Surge current rating.
15) What are the applications of GTO?
16) Define Reverse Recovery Time of SCR.
17) How the GTO differs from a Thyristor?
18) Define reverse recovery time and gate recovery time.
19) Draw the circuit diagram of UJT as an SCR Triggering circuit.
20) What are the two general functions to be full filled by the gate control circuit?
21) What do you mean by commutation?
22) What is Natural commutation and where it is used?

LONG QUESTIONS

1. Draw the four layer structure of SCR.
2. Explain the Two Transistor Analogy of SCR.
3. With neat diagram explain the dynamic characteristic of SCR.
4. Explain the operation, construction of SCR and draw its V-I characteristics curve.
5. Describe the different modes of operation of SCR.
6. Describe light triggering and temperature triggering methods of SCR.
7. Discuss two transistor model of Thyristor. Derive an expression for anode current.
8. Explain **Thermal** triggering and **Radiation** (light) triggering of an SCR.
9. Draw layer diagram of SCR & explain the operation, construction & application of it.
10. Explain operation, construction of SCR & draw V-I characteristics curve.
11. Define commutation and explain briefly about different TURN ON methods of SCR.
12. Enumerate various mechanisms by which Thyristors can be **Triggered** into conduction mode. Discuss these techniques which result in random turn on of a Thyristor?
13. Explain the operation, construction & application of Power Diode.
14. Explain Turn-ON & Turn-OFF behavior of power diode with V and I waveforms.
15. Discuss about the operation of power BJT.
16. Explain operation, construction of power MOSFET & list of application of it.
17. Explain the constructional details and working of low power MOSFET and bring out difference between low power MOSFET and High power MOSFET.
18. Explain the operation, construction of DIAC and draw V-I characteristic.
19. With necessary diagram describe the working of DIAC.
20. Explain construction, operation & V-I characteristics of DIAC. Write use.
21. Explain operation, construction of TRIAC & draw V-I characteristics.
22. Explain different operation mode, construction of TRIAC & its V-I curve.
23. Describe the working of a GTO.
24. Write short notes on GTO and its Applications.
25. Explain the construction, operation of GTO and draw its V-I characteristics curve.
26. Explain the operation, construction of GTO with a neat circuit diagram
27. Explain operation, construction of GTO and draw characteristics curve.
28. Explain the operation & construction of IGBT and its application.
29. Explain the operation, construction of IGBT and draw V-I characteristic.
30. Explain operation, construction of IGBT & draw its characteristics curve.
31. Explain the **R**-Firing, **R-C** firing and **Ramp** Triggering circuit briefly.
32. Draw **UJT** pulse trigger circuit and explain.
33. Describe the general layout diagram of **RC** and **UJT** triggering firing circuit with neat circuit diagram.
34. Describe any one of the **Forced Commutation** technique with neat sketch.
35. Define commutation & explain operation **Resonant Communication** method with neat diagram & waveform.
36. Define commutation & explain working of **Impulse Communication** method with neat diagram & waveforms.
37. Explain **Line Communication** with circuit diagram and waveforms.
38. Explain the **Auxiliary Voltage Commutation** with circuit diagram.

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